EECS 42 – Introduction to Electronics for Computer Science

Midterm Thursday November 6th
In class, Closed Book, Closed Notes, Device Equations Provided
Review Session #1: 5 PM Tuesday Nov 4th, meet at 241 Cory
Review Session #2: 6 PM Wednesday Nov 5th, meet at 241 Cory

Topical Coverage Second Midterm
Schwarz and Oldham Material followed by skills

Chapter 2: all except 2.4 Loop Analysis, 2.6 and 2.7, light on 2.5
Node analysis of circuits with up to 8 branches
Voltage and current dividers

Chapter 3: all
Equivalent circuits: Thevenin and Norton
Nonlinear loads and load lines

Chapter 4: all but only ideal op-amps
Dependent sources, gain, input and output impedance
Ideal Op-Amps
Generalization to Comparators

Chapter 5: all light on 5.3 and no inductor circuits.

Chapter 8.1: Only 8.1
EE 40/42 simple solution method and application to switching and pulses
KCL to get differential equation for capacitor voltage and inductor current

Chapter 10: no flip-flops
Gates and logic functions
Generalization: Timing diagrams

Lectures 15-18, pp. 522-524, 604-611 Logic with state dependent devices
Device I vs. V curves and load line method
Simple inverter and voltage transfer characteristic
Complementary Pull-Up and Pull-Down networks (CMOS)

Likely Exam Emphasis
Analysis of vanilla circuits with dependent sources
Ideal Op-Amps
Analysis of circuits using dependent sources to improve characteristics
Logic Functions and Timing Diagrams
Static but no dynamic analysis of logic gates

$$I_{OUT-SAT-n} = k'_n \left( \frac{W}{L} \right)_n (V_{IN} - V_{Th}) V_{OUT-SAT-n}$$

$$I_{OUT-SAT-p} = k'_p \left( \frac{W}{L} \right)_p (V_{DD} - V_{IN} - |V_{Tp}|) V_{OUT-SAT-p}$$

<table>
<thead>
<tr>
<th></th>
<th>$V_S(V)$</th>
<th>$V_{OUT-SAT}(V)$</th>
<th>$k'(\mu A/V^2)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>0.43</td>
<td>0.63</td>
<td>100</td>
</tr>
<tr>
<td>PMOS</td>
<td>0.4</td>
<td>1</td>
<td>25</td>
</tr>
</tbody>
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For a minimum sized device $W/L = 2$