EECS 42 Introduction to Digital Electronics
Andrew R. Neureuther

These viewgraphs will be handed out in class 10/21/03

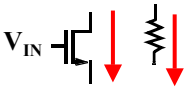
Lecture # 16 Logic with a State Dependent Device

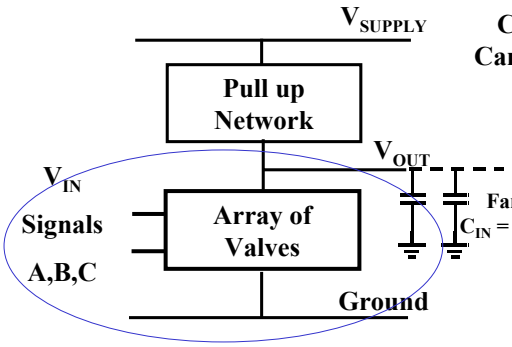
S&O pp. 593-595, 604-606 (read for graphs and not physics or equations), plus Handout of these viewgraphs.

A) State Dependent Device I_{OUT} vs. V_{OUT}
B) Load Line Analysis for Logic Levels
C) Voltage Transfer Characteristics
VTC = plot of V_{OUT} vs. V_{IN}
D) 42S_NMOS Pull-Down Device and Logic

http://inst.EECS.Berkeley.EDU/~ee42/

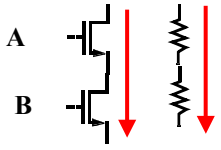
Logic Gates – How are they built in practice?

A Valve is a Transistor 

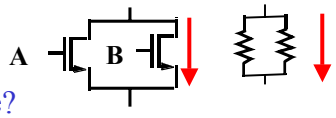


Current flows when V_{IN} is high
Can be modeled by a 10kΩ resistor

Valves in Series => NAND



Valves in Parallel => NOR



What goes in this box?

How does it affect digital performance?

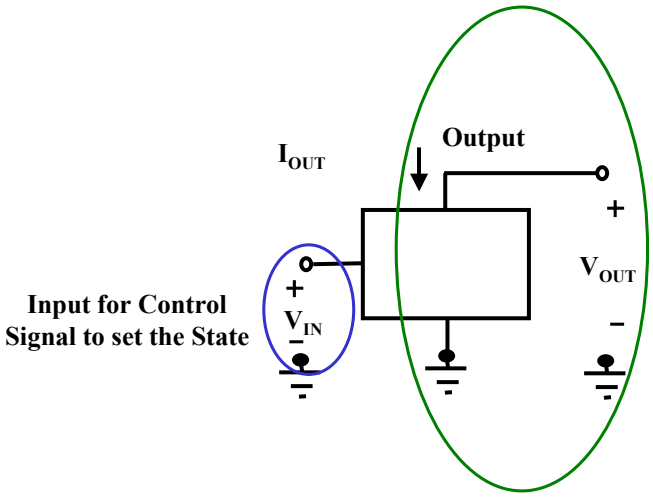
Digital Logic from State-Dependent Three-Terminal Devices

Three-terminal devices such as MOS transistors have output characteristics (such as I_{OUT} vs. V_{OUT} curves) on the output side that can be programmed by changing signals on the input side (such as the input voltage).

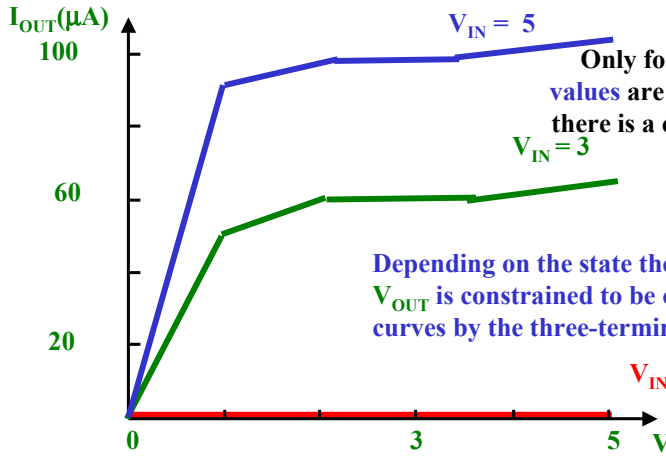
The input voltage V_{IN} can thus be viewed as changing or programming the 'State' of the output of the device.

Three-terminal devices whose input voltage V_{IN} or 'State' can be programmed can be used to make digital logic devices for computers whose outputs respond to input signals.

State-Dependent Three-Terminal Device Element



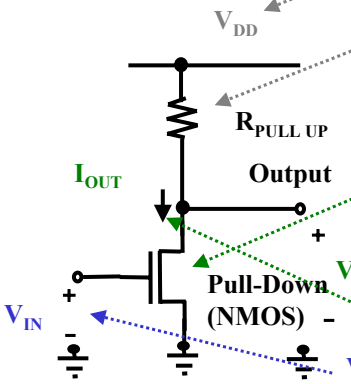
State-Dependent Device I_{OUT} vs. V_{OUT}



Only four states or input values are shown but typically there is a continuum of states.

Depending on the state the output I_{OUT} vs. V_{OUT} is constrained to be on one of these curves by the three-terminal device.

Terminology for a Logic Circuit



V_{DD} = Power supply voltage (D is from Drain) we do not draw the symbol.

Pull-Up Network = Set of devices used to carry current from the power supply to the output node to charge the output node to the power supply voltage.

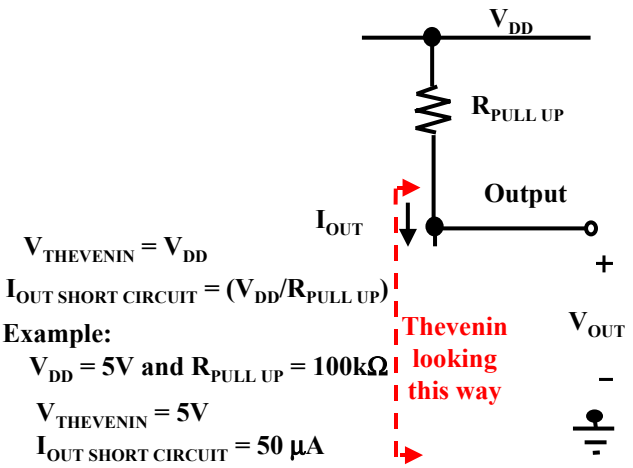
Pull-Down Network = Set of devices used to carry current from the output node to ground to discharge the output node to ground.

I_{OUT} = Current for the device under study.

V_{TD} = Threshold Voltage value of V_{IN} at which the Pull-Down (NMOS transistor) begins to conduct.

$V_{OUT-SAT-D}$ = Value of V_{OUT} beyond which the current I_{OUT-D} saturates at the (drain) current saturation value $I_{OUT-SAT-D}$.

Thevenin Model For Pull-Up Device



$V_{THEVENIN} = V_{DD}$

$I_{OUT\ SHORT\ CIRCUIT} = (V_{DD}/R_{PULL\ UP})$

Example:

$V_{DD} = 5V$ and $R_{PULL\ UP} = 100k\Omega$

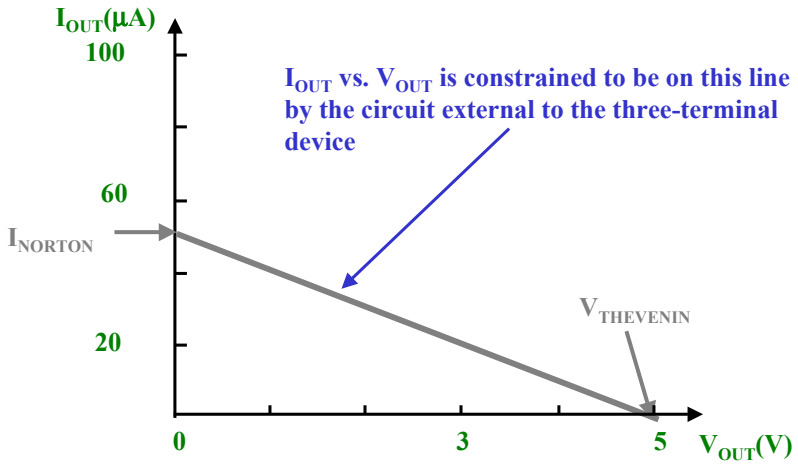
$V_{THEVENIN} = 5V$

$I_{OUT\ SHORT\ CIRCUIT} = 50\ \mu A$

EECS 42 Intro. Digital Electronics, Fall 2003 Lecture 16: 10/21/03 A.R. Neureuther
Version Date 10/18/03

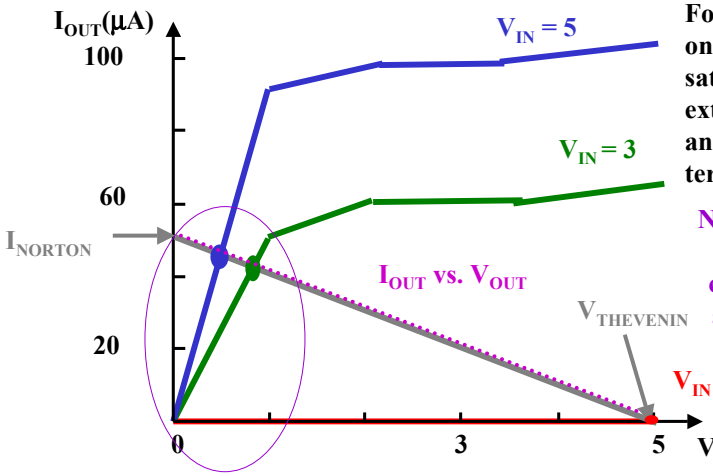
Thevenin Model For Pull-Up Device

I_{OUT} vs. V_{OUT}
For the Pull-Up Resistor and V_{DD}



Composite Current Plot for the Logic Circuit

Three-Terminal Device
Plus Load Line for the Pull-Up Device

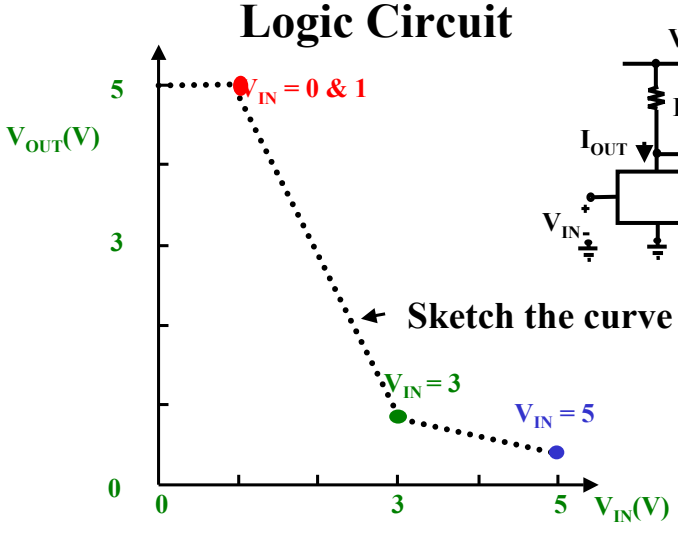


For a given state only one point satisfies both the external circuit and the three-terminal device

Note that when V_{OUT} is low current flows and power is consummed

EECS 42 Intro. Digital Electronics, Fall 2003 Lecture 16: 10/21/03 A.R. Neureuther
Version Date 10/18/03

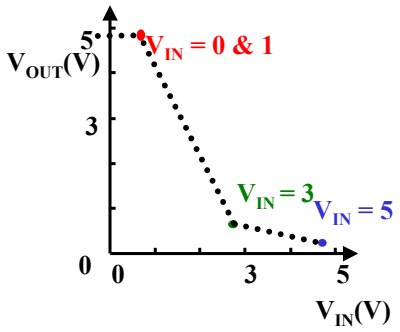
Voltage Transfer Function for the Logic Circuit



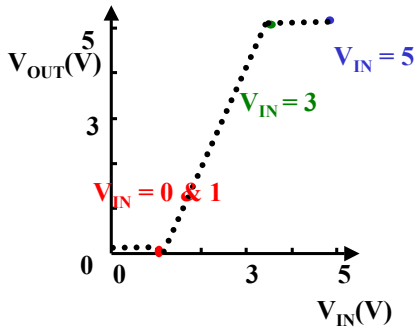
Voltage Transfer Function: V_{OUT} vs. V_{IN}

The V_{OUT} vs. V_{IN} characteristic is another view of the logic gate that is used to determine the inverting and noninverting nature of a gate.

Inverting type



Noninverting type



Saturation Current 42S_NMOS Model

Current I_{OUT} only flows when V_{IN} is larger than the threshold value V_{TD} and the current is proportional to V_{OUT} up to $V_{OUT-SAT-D}$ where it reaches the saturation current

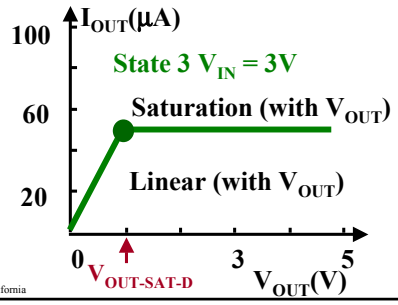
$$I_{OUT-SAT-D} = k_D\left(V_{IN} - V_{TD}\right)V_{OUT-SAT-D}$$

Note that we have added an extra parameter to distinguish between threshold (V_{TD}) and saturation ($V_{OUT-SAT-D}$).

Example:
k_D = 25 μA/V²
V_{TD} = 1V
$V_{OUT-SAT-D}$ = 1V

Use these values in the homework.

$$I_{OUT-SAT-PD} = 25\frac{\mu A}{V^2}(3V - 1V)1V = 50\mu A$$



Drawing I_{OUT} as function of V_{IN} and V_{OUT} for the 42S_NMOS Pull-Down Device

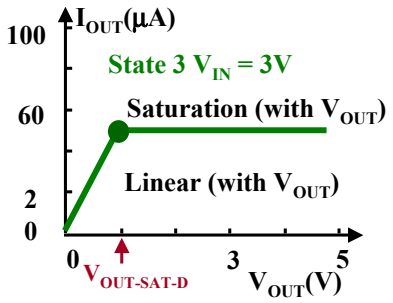
The equations are expressly designed for EE42 to make it very simple to draw I_{OUT} vs. V_{OUT}

1) For $V_{IN} < V_{TD}$, the current is zero.

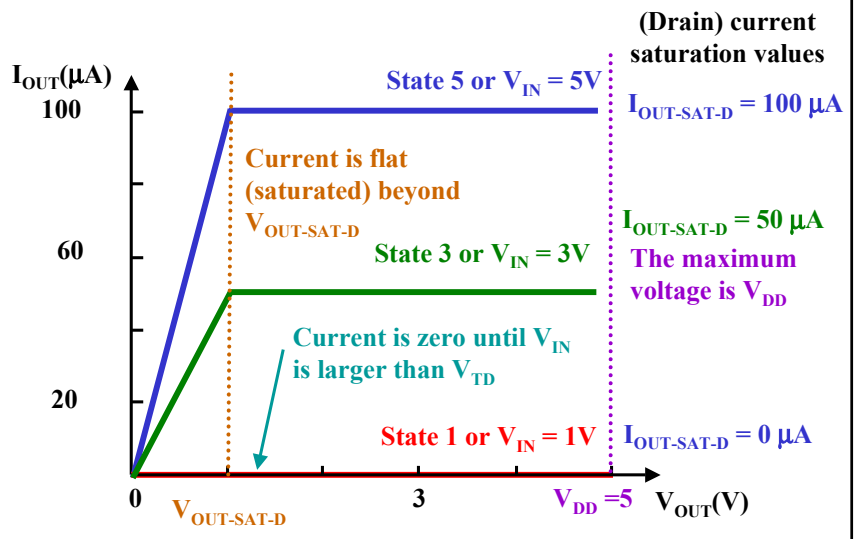
2) For $V_{IN} > V_{TD}$, first evaluate the current I_{OUT} at $V_{OUT} = V_{OUT\text{-}SAT\text{-}D}$ and plot the single point (I_{OUT}, V_{OUT})

3) Draw a line from this point to the origin to create the linear region.

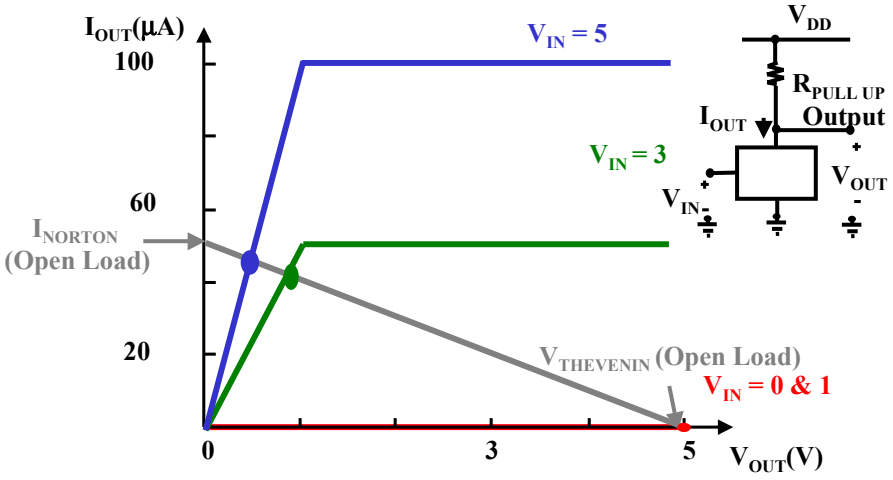
4) Draw a horizontal line from this point to create the saturation region



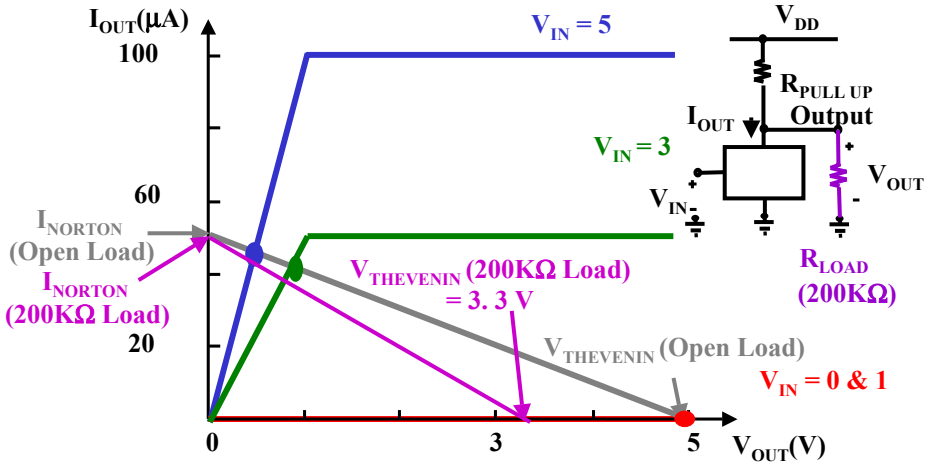
States of 42S_NMOS are Voltage Levels of V_{IN}



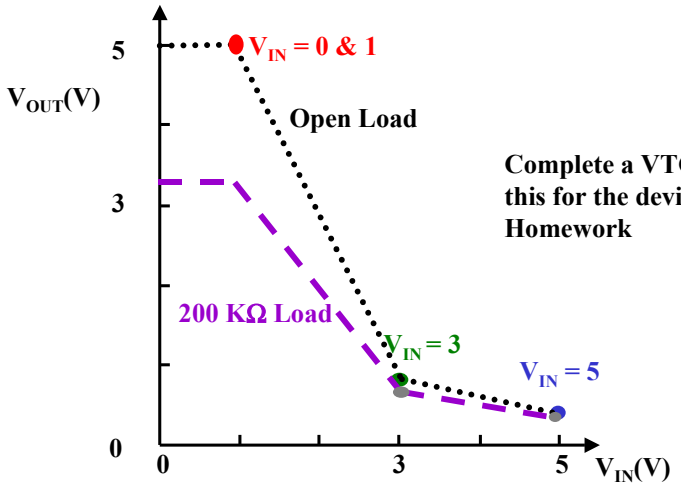
Composite Current Plot for the 42S_NMOS Logic Circuit



Composite Current Plot for the 42S_NMOS Circuit with 200kΩ Load to Ground



Voltage Transfer Function for the 42S_NMOS Logic Circuit w/wo Load



Complete a VTC like this for the device in the Homework