

EECS 42 Introduction Digital Electronics

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These viewgraphs will be handed out in class.

Lecture # 17 Logic with Complementary Devices
S&O pp. 607-611 (read for graphs and not physics or equations),
plus Handout of Wed Lectures.

A) Discovering a Pull-Up Device

B) Designing a Pull-Up Device

C) EE 42 Pull-Up Device Model (42S_P MOS)

D) Composite I_{OUT} vs. V_{OUT}

E) Voltage Transfer Function and V_{MID}

<http://inst.EECS.Berkeley.EDU/~ee42/>

Problems and Opportunities in Logic Circuit Design

Problem #1: Significant wasted current and power when V_{OUT} is low.

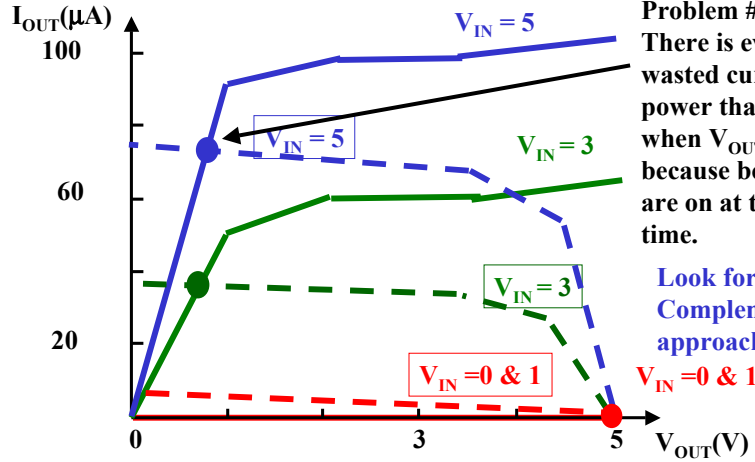
Problem #2: High value of V_{OUT} is adversely affected by a load resistor.

Missed Opportunity: The value of the input control signal is not used to adjust the state of the pull-up device.

What if : If the pull-up device could be a state-dependent device what kind of device would we want?

Pull-Up Device Design: Graphical Trial #1

Similar pull-up and pull-down states

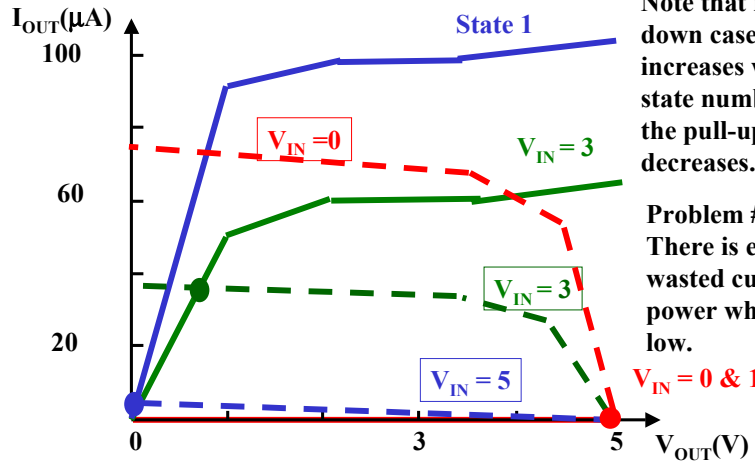


Problem #1 is worse!
 There is even more wasted current and power than before when V_{OUT} is low because both devices are on at the same time.

Look for a more Complementary approach.

Pull-Up Device Design: Trial 2

Complementary pull-up and pull-down states



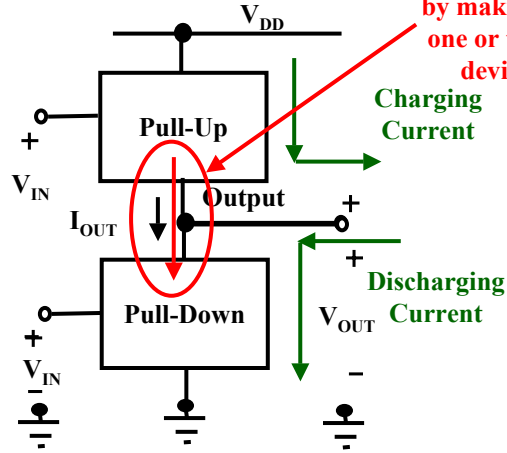
Note that in the pull-down case the current increases with the state number and in the pull-up case it decreases.

Problem #1 is solved.
 There is essentially no wasted current or power when V_{OUT} is low.

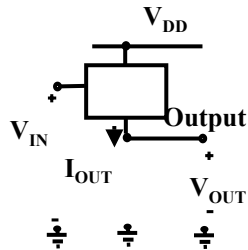
Pull-Down and Pull-Up Must Complement Rather Than Fight Each Other

Reduce the Short-Circuit Current by making either one or the other device off.

Input for State Control Signal
Share Same Signal
Input for State Control Signal



Desirable Complementary Device Characteristics

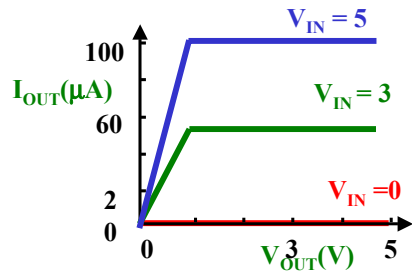


We desire characteristics that are **complementary** for the pull-down and pull-up state-dependent devices.

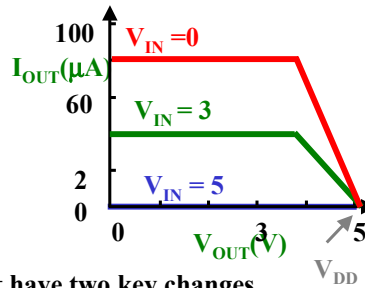
V_{IN}	Low	High
Pull-Down Current	Low not leak	High Discharge Output
Pull-Up Current	High Charge Output	Low not leak

Designing the Complementary Device

Make This



Into This

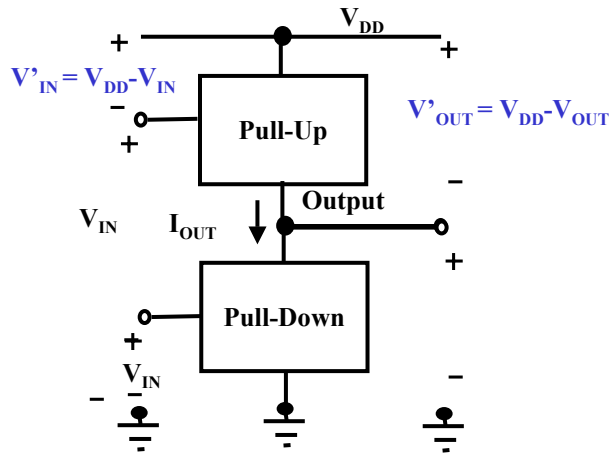
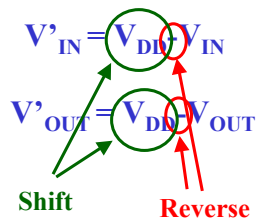


The curve sets are very similar but have two key changes.

The creation of current with input State (V_{IN}) is reverse ordered (and also shifted).

The dependence on V_{OUT} is reversed in sign and shifted by V_{DD}

Pull-Up Can be viewed as Complementary by using Device rather than Circuit voltages $V_{DD}-V_X$



Saturation Current NMOS Model

Current I_{OUT} only flows when V_{IN} is larger than the threshold value V_{TD} and the current is proportional to V_{OUT} up to $V_{OUT-SAT-D}$ where it reaches the saturation current

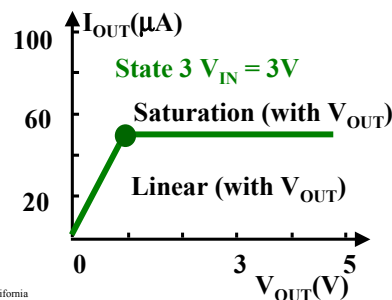
$$I_{OUT-SAT-D} = k_D (V_{IN} - V_{TD}) V_{OUT-SAT-D}$$

Note that we have added an extra parameter to distinguish between threshold (V_{TD}) and saturation ($V_{OUT-SAT-D}$).

Example:

$k_D = 25 \mu A/V^2$ Use these
 $V_{TD} = 1V$ values in the
 $V_{OUT-SAT-D} = 1V$ homework.

$$I_{OUT-SAT-PD} = 25 \frac{\mu A}{V^2} (3V - 1V) 1V = 50 \mu A$$



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Saturation Current 42S_PMOS Model

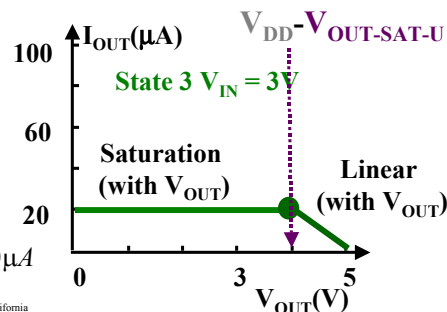
Current I_{OUT} only flows when V_{IN} is smaller than V_{DD} by the threshold value V_{TU} (that is $V_{DD} - V_{IN} > V_{TU}$) and the current is proportional to the excess gate voltage ($V_{DD} - V_{IN} - V_{TU}$) and is also proportional to ($V_{DD} - V_{OUT}$) above ($V_{DD} - V_{OUT-SAT-U}$) where it has its maximum saturated value.

$$I_{OUT-SAT-U} = k_U (V_{DD} - V_{IN} - V_{TU}) V_{OUT-SAT-U}$$

Example:

$k_U = 20 \mu A/V^2$ Use these
 $V_{TU} = 1V$ values in the
 $V_{OUT-SAT-U} = 1V$ homework.

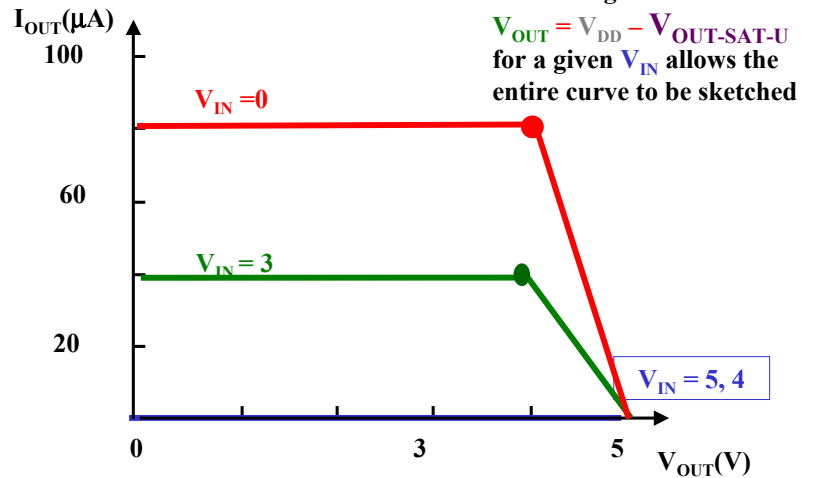
$$I_{OUT-SAT-U} = 20 \frac{\mu A}{V^2} (5V - 3V - 1V) 1V = 20 \mu A$$



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42S_PMOS Pull-UP Device Curves

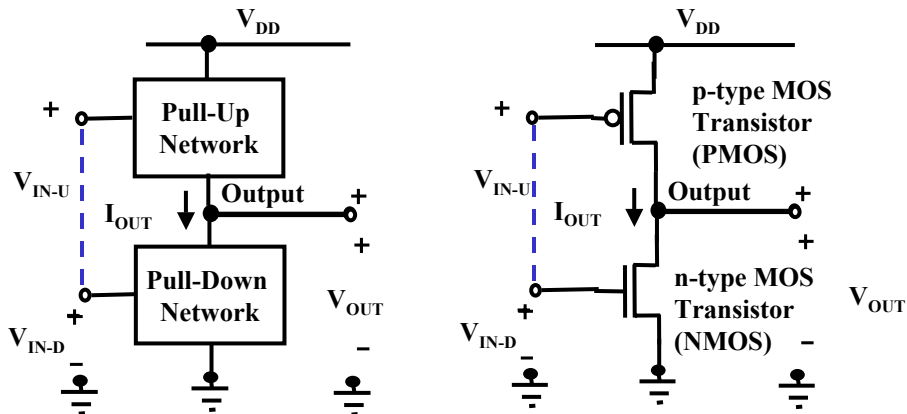
I_{OUT} vs. V_{OUT}



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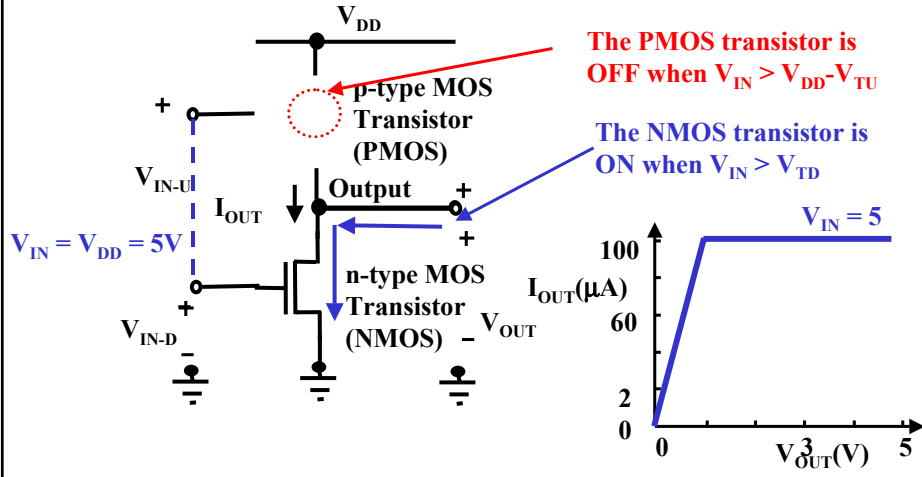
Transistor Inverter Example

It may be simpler to just **think of PMOS and NMOS transistors** instead of a general 3 terminal pull-up or pull-down devices or networks.

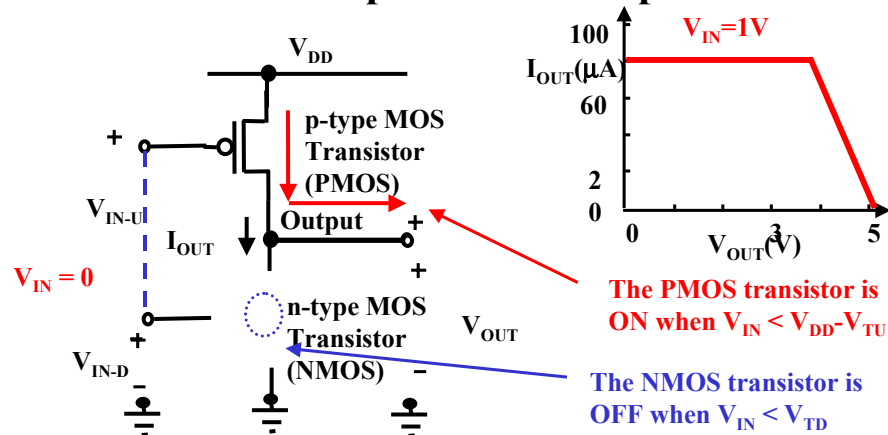


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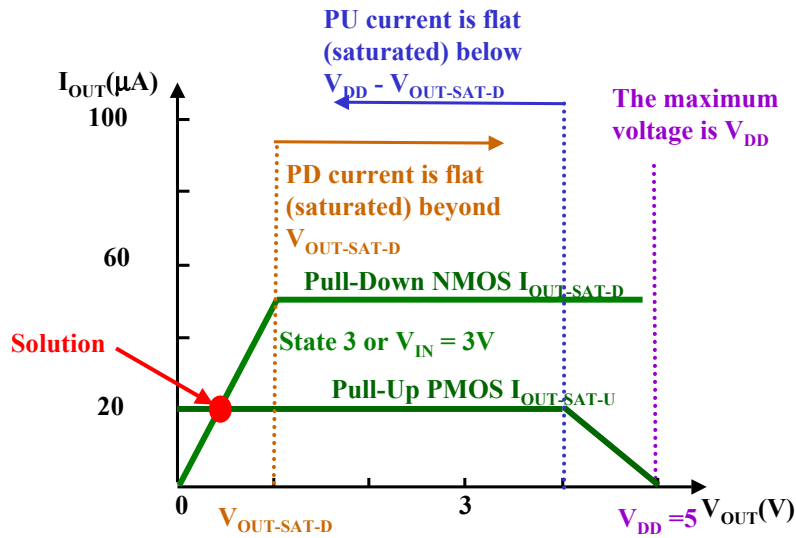
Case #1: $V_{IN} = V_{DD} = 5V$ The Output is Pulled-Down



Case #2: $V_{IN} = 0$ The Output is Pulled-Up

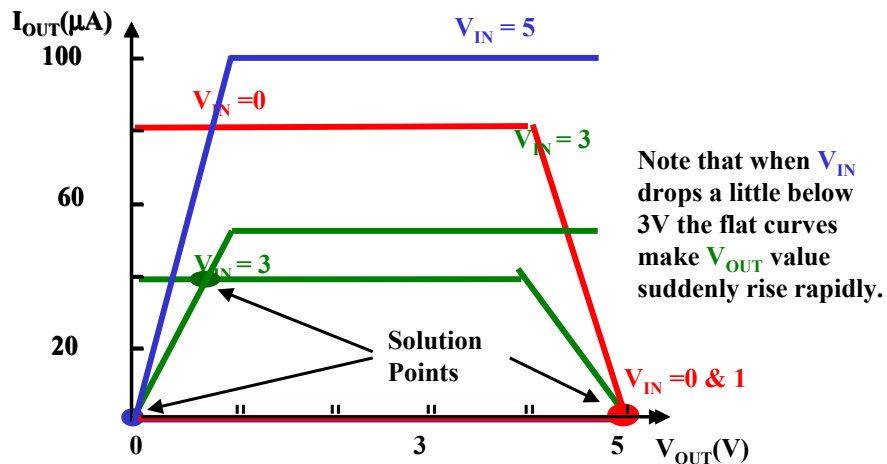


Composite I_{OUT} vs. V_{OUT} for CMOS



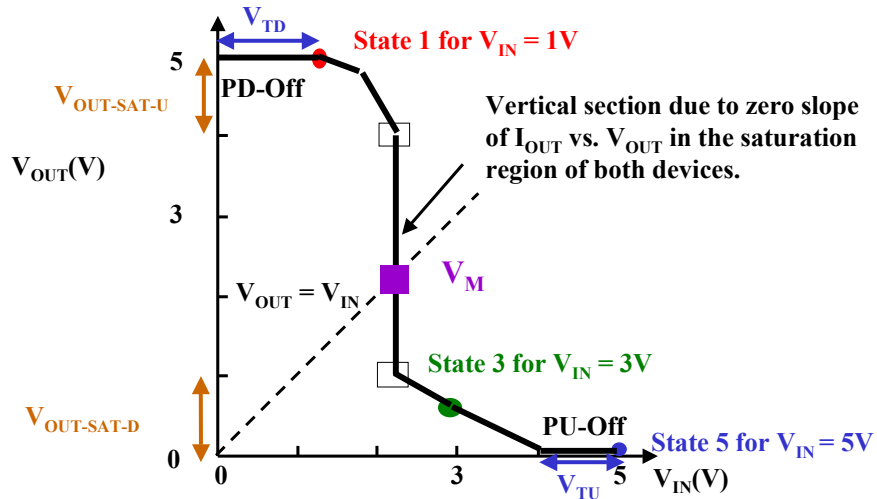
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Composite I_{OUT} vs. V_{OUT} to Find Points That Satisfies Both Devices for Each V_{IN}



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Voltage Transfer Function for the Complementary Logic Circuit



Method for Finding V_M

At V_M ,

- 1) $V_{OUT} = V_{IN} = V_M$
- 2) Both devices are in saturation
- 3) $I_{OUT-SAT-D} = I_{OUT-SAT-U}$

$$I_{OUT-SAT-D} = k_D (V_{IN} - V_{TD})^2 V_{OUT-SAT-D}$$

$$= I_{OUT-SAT-U} = k_U (V_{DD} - V_{IN} - V_{TU})^2 V_{OUT-SAT-U}$$

Substitute V_M

Solve for V_M

Example Result: When $k_D = k_U$, $V_{OUT-SAT-D} = V_{OUT-SAT-U}$
and $V_{TD} = V_{TU}$, then $V_M = V_{DD}/2$