Problems and Opportunities in Logic Circuit Design

Problem #1: Significant wasted current and power when V<sub>OUT</sub> is low.
Problem #2: High value of V<sub>OUT</sub> is adversely affected by a load resistor.

Missed Opportunity: The value of the input control signal is not used to adjust the state of the pull-up device.

What if: If the pull-up device could be a state-dependent device what kind of device would we want?

Pull-Up Device Design: Graphical Trial #1

Similar pull-up and pull-down states

Problem #1 is worse! There is even more wasted current and power than before when V<sub>OUT</sub> is low because both devices are on at the same time. Look for a more Complementary approach.

Pull-Up Device Design: Trial 2

Complementary pull-up and pull-down states

Note that in the pull-down case the current increases with the state number and in the pull-up case it decreases.

Desirable Complementary Device Characteristics

We desire characteristics that are complementary for the pull-down and pull-up state-dependent devices.
Designing the Complementary Device

Make This Into This

\[ V_{OUT}(V) = 0, 3, 5 \]

\[ V_{IN} = 0 \]

\[ I_{OUT} (\mu A) \]

\[ 0 \quad 20 \quad 60 \quad 100 \]

\[ V_{IN} = 3 \]

The curve sets are very similar but have two key changes.

The creation of current with input State \(V_{IN}\) is reverse ordered (and also shifted).

The dependence on \(V_{OUT}\) is reversed in sign and shifted by \(V_{DD}\).

The Saturation Current NMOS Model

Current \(I_{OUT}\) only flows when \(V_{IN}\) is larger than the threshold value \(V_{TD}\) and the current is proportional to \(V_{OUT}\) up to \(V_{OUT-SAT-D}\) where it reaches the saturation current:

\[ I_{OUT-SAT-D} = k_D (V_{IN} - V_{TD}) \]

\[ V_{OUT}(V) \]

\[ I_{OUT}(\mu A) \]

\[ 0 \quad 20 \quad 60 \quad 100 \]

\[ V_{IN} = 3 \]

\[ V_{IN} = 5 \]

\[ \frac{25 \mu A}{V^2} \]

Use these values in the homework.

\[ \frac{1}{2} (V' - V'') \]

Linear (with \(V_{OUT}\))

Saturation (with \(V_{OUT}\))

Example:

\[ k_D = \frac{25 \mu A}{V^2} \]

\[ V_{TD} = 1V \]

\[ V_{OUT-SAT-D} = 1V \]

Evaluating the current when \(V_{OUT} = V_{DD} - V_{OUT-SAT-U}\) for a given \(V_{IN}\) allows the entire curve to be sketched.

The Transistor Inverter Example

It may be simpler to just think of PMOS and NMOS transistors instead of a general 3 terminal pull-up or pull-down devices or networks.
Case #1: \( V_{IN} = V_{DD} = 5V \)
The Output is Pulled-Down

\[ V_{OUT} \]

\[ I_{OUT} \]

Output

\[ V_{IN-D} \]
\[ V_{DD} \]
\[ V_{IN-U} \]

p-type MOS Transistor (PMOS)

n-type MOS Transistor (NMOS)

\[ V_{IN} = V_{DD} = 5V \]
The PMOS transistor is OFF when \( V_{IN} > V_{DD} - V_{TU} \)
The NMOS transistor is ON when \( V_{IN} = V_{TD} \)

Composite \( I_{OUT} \) vs. \( V_{OUT} \) for CMOS

PU current is flat (saturated) below \( V_{IN} \times V_{OUT-SAT-D} \)

PD current is flat (saturated) beyond \( V_{OUT-SAT-D} \)

Solution

\( V_{OUT}(V) \)

\( I_{OUT}(\mu A) \)

0

20

60

100

0

3

V_{IN} = V_{DD} = 5V

State 1 for \( V_{IN} = 1V \)
Vertical section due to zero slope
of \( I_{OUT} \) vs. \( V_{OUT} \) in the saturation region of both devices.

State 3 for \( V_{IN} = 3V \)

State 5 for \( V_{IN} = 5V \)

\( V_{OUT-SAT-D} \)

\( V_{OUT-SAT-U} \)

Pull-Up PMOS \( I_{OUT-SAT-U} \)

Pull-Down NMOS \( I_{OUT-SAT-D} \)

\( V_{DD} \)

\( V_{IN} \)

\( V_{OUT} \)

Voltage Transfer Function for the Complementary Logic Circuit

At \( V_{M} \):
1) \( V_{OUT} = V_{IN} = V_{M} \)
2) Both devices are in saturation
3) \( I_{OUT-SAT-D} = I_{OUT-SAT-U} \)

\[ I_{OUT-SAT-D} = k_{D} (V_{IN} - V_{TD}) \]
\[ = k_{D} (V_{TD} - V_{OUT-SAT-D}) \]

\[ I_{OUT-SAT-U} = k_{P} (V_{OD} - V_{IN} - V_{TD} - V_{OUT-SAT-D}) \]

Substitute \( V_{M} \)

Solve for \( V_{M} \)

Example Result: When \( k_{D} = k_{P} \), \( V_{OUT-SAT-D} = V_{OUT-SAT-U} \)
and \( V_{OD} = V_{TD} \), then \( V_{M} = V_{OD}/2 \)