EECS 42 Introduction Digital Electronics
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Quiz 10/30 and Midterm 10/6

Lecture # 18 Logic Transients (Handout)

A) Review:Quiz 10/30 and Midterm 11/6
B) Transient as Capacitor Charging
C) Equivalent Resistance for MOS
D) Inverter Propagation Delay
E) Complementary MOS Operation

http://inst.EECS.Berkeley.EDU/~ee42/

Midterm #2 Coverage

- Logic Functions and Timing Diagrams ← Quiz 10/30
- Analysis of vanilla circuits with dependent sources
- Ideal Op-Amps
- Analysis of circuits using dependent sources to improve characteristics
- Static analysis of logic gates

	V_T(V)	$V_{OUT-SAT}$(V)	k'(μA/V²)
NMOS	0.43	0.63	100
PMOS	0.4	1	25

Minimum sized devices have W/L = 2

$$I_{OUT-SAT-n} = k_n'\left(\frac{W}{L}\right)_n (V_{IN} - V_{Tn})V_{OUT-SAT-n}$$

$$I_{OUT-SAT-p} = k_p'\left(\frac{W}{L}\right)_p (V_{DD} - V_{IN} - |V_{Tp}|)V_{OUT-SAT-p}$$

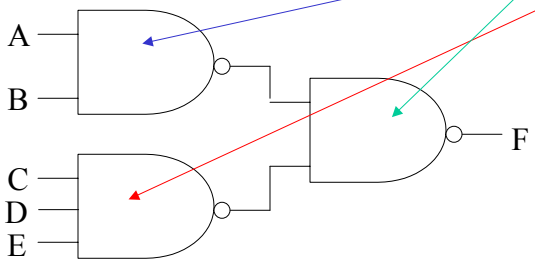
Logical Synthesis
Guided by DeMorgan's Theorem

DeMorgan's Theorem :

$$A + B + C = \overline{[\overline{A}\,\overline{B}\,\overline{C}]} \quad \text{or} \quad \overline{A} + \overline{B} + \overline{C} = \overline{[A\,B\,C]}$$

Example of Using DeMorgan's Theorem:

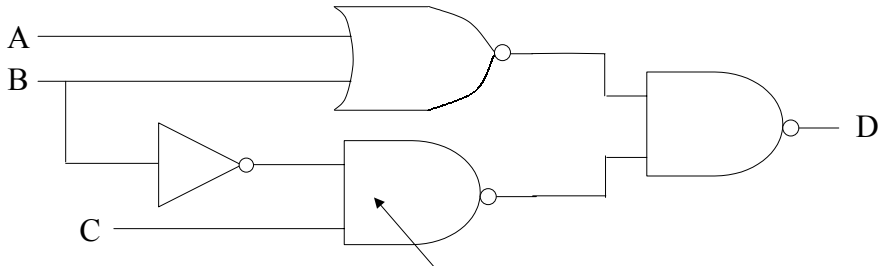
$$F = A \bullet B + C \bullet D \bullet E = \overline{AB} \bullet \overline{CDE}$$



Thus any sum of products expression can be immediately synthesized from NAND gates alone

EFFECT OF GATE DELAY

Cascade of Logic Gates



Inputs have different delays, but we ascribe a single worst-case delay τ to every gate

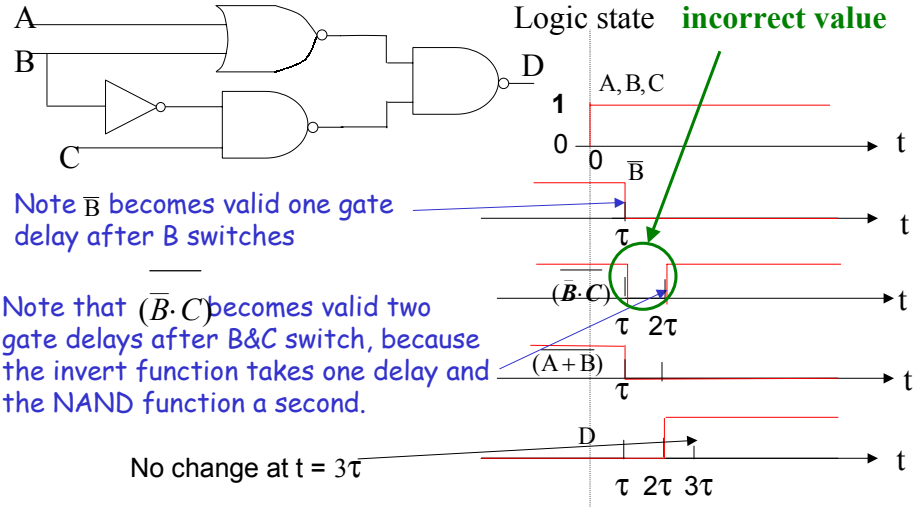
How many "gate delays for shortest path? ANSWER : 2

How many gate delays for longest path? ANSWER : 3

TIMING DIAGRAMS

Show transitions of variables vs time

Glitching: temporary switching to an incorrect value



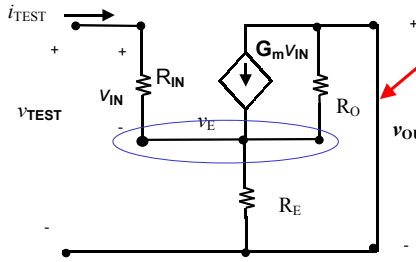
Note $\overline{B}$ becomes valid one gate delay after B switches

Note that $(\overline{B \cdot C})$ becomes valid two gate delays after B&C switch, because the invert function takes one delay and the NAND function a second.

No change at t = 3τ

EXAMPLE CIRCUIT: INCREASED INPUT RESISTANCE

Add resistor R_E



The output has been assumed to be shorted

$v_{OUT} = 0$

Analysis: apply i_{TEST} and evaluate v_{TEST}

$$v_{IN} = R_{IN} i_{TEST} \qquad v_{TEST} = R_{IN} i_{TEST} + v_E$$

Similar to the homework

KCL

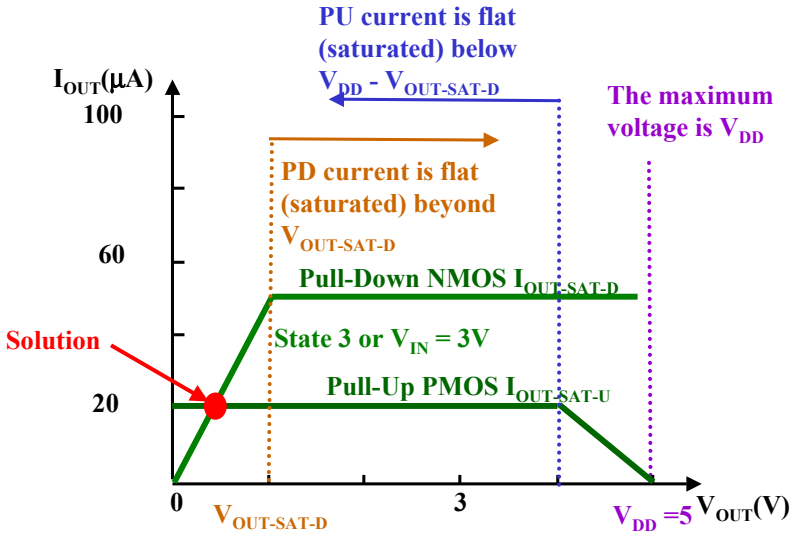
$$\frac{v_E}{R_E} + \frac{v_E}{R_0} - i_{TEST} - G_m R_{IN} i_{TEST} = 0$$

Check for special case for R_0 infinite

$$\frac{v_{TEST}}{i_{TEST}} = R_{IN} + (1 + G_m R_{IN}) R_E$$

Intuitive Explanation: R_E puts R_{IN} on a node whose voltage increases in response to current in R_{IN}.

Composite I_{OUT} vs. V_{OUT} for CMOS



Method for Finding V_M

At V_M,

1) $V_{OUT} = V_{IN} = V_M$
2) Both devices are in saturation
3) $I_{OUT-SAT-D} = I_{OUT-SAT-U}$

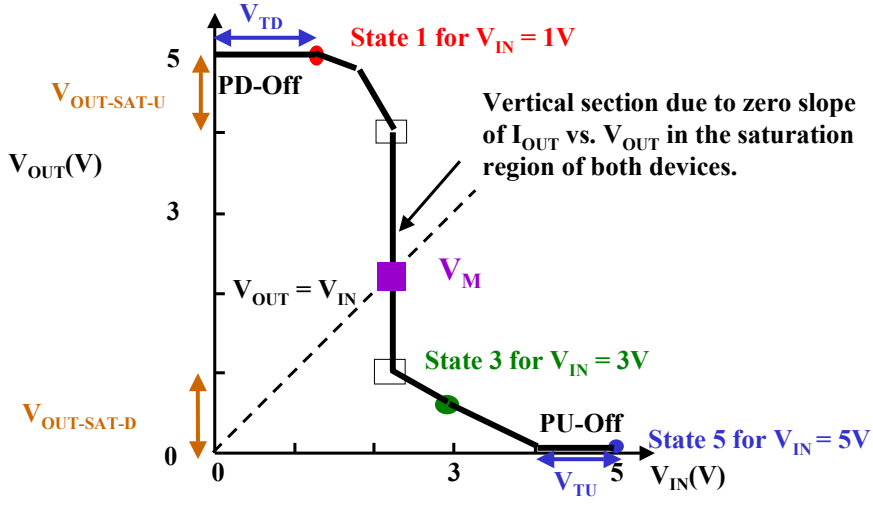
$$I_{OUT-SAT-D} = k_D\left(V_{IN} - V_{TD}\right)V_{OUT-SAT-D}$$
$$= I_{OUT-SAT-U} = k_U\left(V_{DD} - V_{IN} - V_{TU}\right)V_{OUT-SAT-U}$$

Substitute V_M

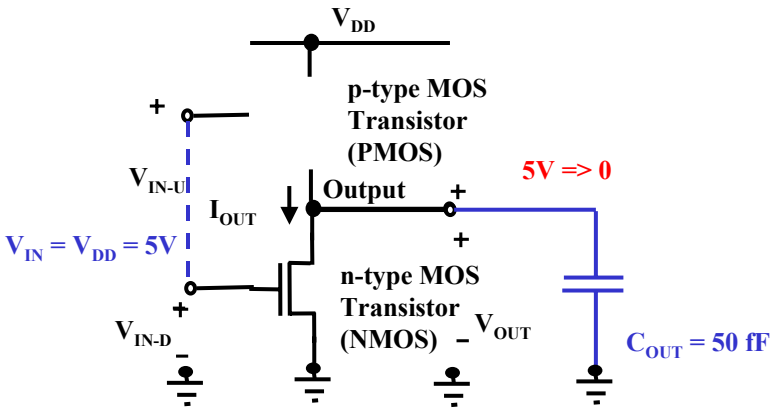
Solve for V_M

Example Result: When $k_D = k_P$, $V_{OUT-SAT-D} = V_{OUT-SAT-U}$ and $V_{TD} = V_{TU}$, then $V_M = V_{DD}/2$

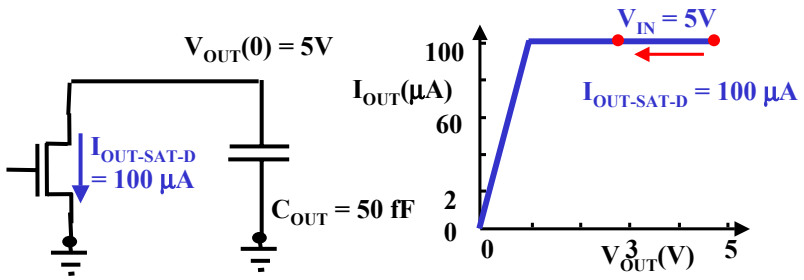
Voltage Transfer Function for the Complementary Logic Circuit



Transient Gate Problem: Discharging and Charging Capacitance on the Output



Output Propagation Delay High to Low

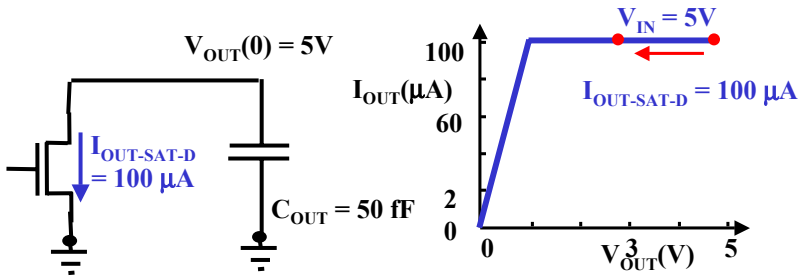


When V_{IN} goes High V_{OUT} starts decreases with time

Assume that the necessary voltage swing to cause the next downstream gate to begin to switch is $V_{DD}/2$ or 2.5V.

That is the propagation delay τ_{HL} for the output to go from high to low is the time to go from V_{DD} = 5V to to $V_{DD}/2$ =2.5V

Output Propagation Delay High to Low (Cont.)



When $V_{OUT} > V_{OUT-SAT-D}$ the available current is $I_{OUT-SAT-D}$

For this circuit when $V_{OUT} > V_{OUT-SAT-D}$ the available current is constant at $I_{OUT-SAT-D}$ and the capacitor discharges.

The propagation delay is thus

$$\Delta t = \frac{C_{OUT}\Delta V}{I_{OUT-SAT-D}} = \frac{C_{OUT}V_{DD}}{2I_{OUT-SAT-D}} = \frac{50\,fF \cdot 2.5V}{100\mu A} = 1.25ns$$

Switched Equivalent Resistance Model

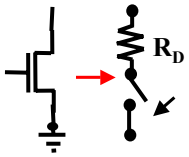
The above model assumes the device is an ideal constant current source.

1) This is not true below $V_{OUT\text{-}SAT\text{-}D}$ and leads to in accuracies.

2) Combining ideal current sources in networks with series and parallel connections is problematic.

Instead define an equivalent resistance for the device by setting $0.69R_DC$ equal to the Δt found above

$$\Delta t = \frac{C_{OUT}V_{DD}}{2I_{OUT-SAT-D}} = 0.69R_DC_{OUT}$$

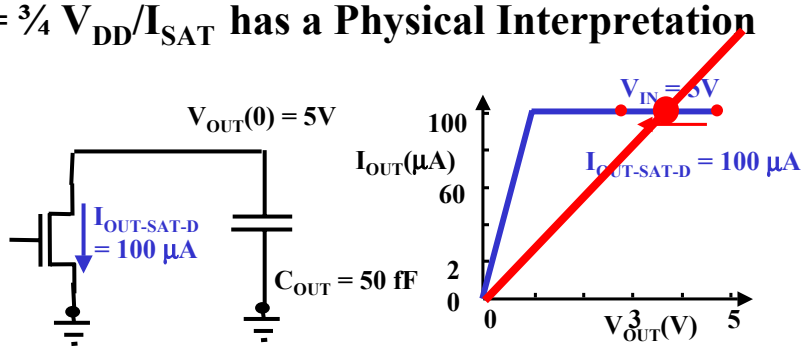


This gives

$$R_D = \frac{V_{DD}}{2\cdot(0.69)I_{OUT-SAT-D}} \approx \frac{3}{4}\frac{V_{DD}}{I_{OUT-SAT-D}} = \frac{3}{4}\frac{5V}{100\mu A} = 37.5k\Omega$$

Each device can now be replaced by this equivalent resistor.

$R_D = ¾\ V_{DD}/I_{SAT}$ has a Physical Interpretation



¾ V_{DD} is the average value of V_{OUT}

Approximate the NMOS device curve by a straight line from (0,0) to ($I_{OUT\text{-}SAT\text{-}D}$, ¾ V_{DD}).

Interpret the straight line as a resistor with

$$\text{slope} = 1/R = ¾\ V_{DD}/I_{SAT}$$

Switched Equivalent Resistance Values

The resistor values depend on the properties of silicon, geometrical layout, design style and technology node.

n-type silicon has a carrier mobility that is 2 to 3 times higher than p-type.

The resistance is inversely proportion to the gate width/length in the geometrical layout.

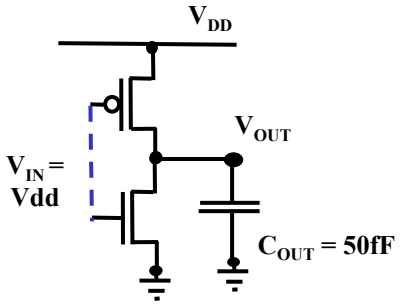
Design styles may restrict all NMOS and PMOS to be of a predetermined fixed size.

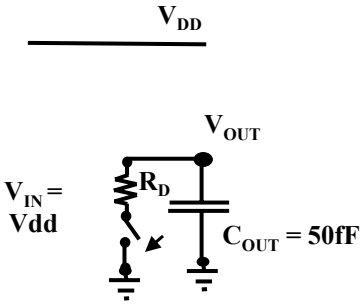
The current per unit width of the gate increases nearly inversely with the linewidth.

For convenience in EE 42 we assume
$R_D = R_U = 10\ k\Omega$ for $V_{DD} = 5V$ and
$R_D = R_U = 10\ k\Omega$ for $V_{DD} = 5V$

Inverter Propagation Delay

Discharge (pull-down)





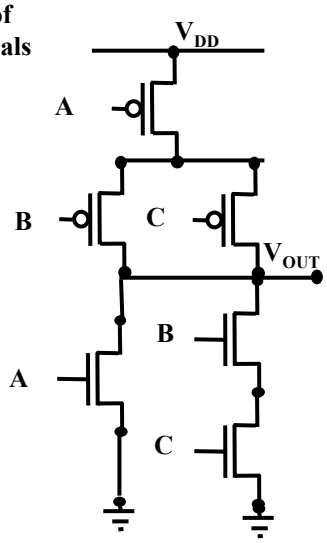
$\Delta t = 0.69 R_D C_{OUT} = 0.69(10k\Omega)(50fF) = 345$ ps

Discharge (pull-up)

$\Delta t = 0.69 R_U C_{OUT} = 0.69(10k\Omega)(50fF) = 345$ ps

CMOS Logic Gate

NMOS and PMOS use the same set of input signals



PMOS only in pull-up

PMOS conduct when input is low

PMOS do not conduct when A +(BC)

NMOS only in pull-down

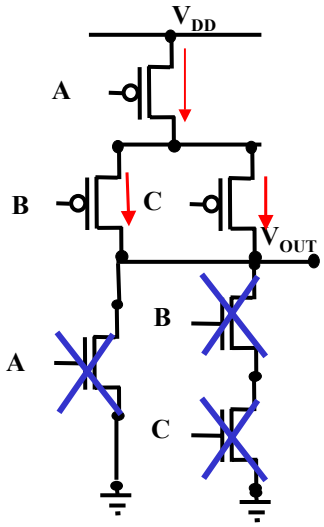
NMOS conduct when input is high.

NMOS conduct for A + (BC)

Logic is Complementary and produces $F = \overline{A + (BC)}$

CMOS Logic Gate: Example Inputs

A = 0
B = 0
C = 0



PMOS all conduct

Output is High

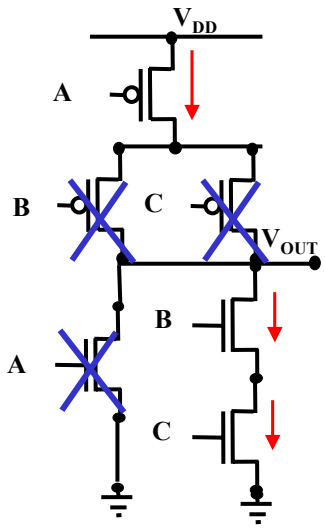
$= V_{DD}$

NMOS do not conduct

Logic is Complementary and produces F = 1

CMOS Logic Gate: Example Inputs

A = 0
B = 1
C = 1



PMOS A conducts; B and C Open

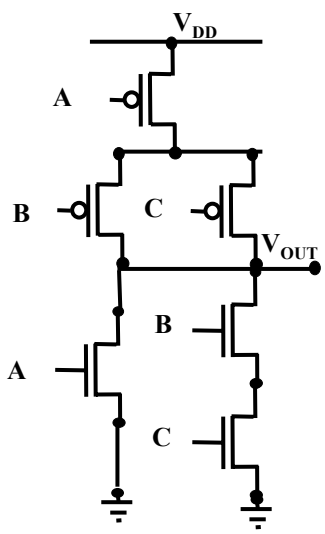
Output is High

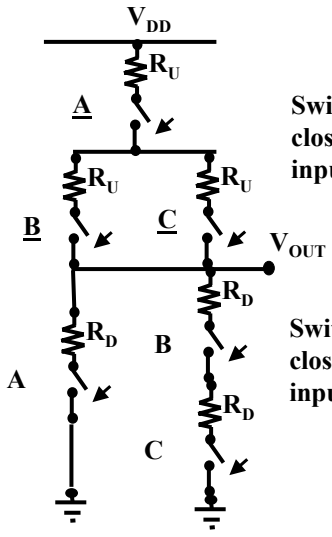
= 0

NMOS B and C conduct; A open

Logic is Complementary and produces F = 0

Switched Equivalent Resistance Network





Switches close when input is low.

Switches close when input is high.