Lecture # 19 Logic Transients
Handout of Wed Lecture.

A) Quiz
B) Worst Case CMOS Delay
C) Delay in CMOS Cascade

http://inst.EECS.Berkeley.EDU/~ee42/

2nd Midterm 11/6 See Coverage Sheet

CASCADE OP-AMP CIRCUITS

How do you get started on finding $V_O$?

Hint: Identify Stages

Hint: $I_{IN}$ does not affect $V_{O1}$

See the further examples of op-amp circuits in the reader
Composite Current Plot for the 42S_NMOS Circuit with 200kΩ Load to Ground

VIN = 0 & 1

VOUT(V)

IOUT(µA)

20

60

100

VIN = 3

VIN = 5

VDD

RLOAD (200KΩ)

RPULL UP Output

INORTON (Open Load)

I_{NORTH} (200KΩ Load)

V_{THEVENIN} (200KΩ Load) = 3.3 V

V_{THEVENIN} (Open Load)

V_{OUT} = 0 & 1

VIN

Solution

State 3 or VIN = 3V

Pull-Down NMOS I_{OUT-SAT-D}

PD current is flat (saturated) beyond V_{OUT-SAT-D}

Pull-Up PMOS I_{OUT-SAT-U}

PU current is flat (saturated) below V_{DD} - V_{OUT-SAT-D}

The maximum voltage is V_{DD}

V_{DD} = 5V

V_{OUT}
When $V_{OUT} > V_{OUT-SAT-D}$ the available current is $I_{OUT-SAT-D}$

For this circuit when $V_{OUT} > V_{OUT-SAT-D}$ the available current is constant at $I_{OUT-SAT-D}$ and the capacitor discharges.

The propagation delay is thus

$$\Delta t = \frac{C_{OUT}\Delta V}{I_{OUT-SAT-D}} = \frac{C_{OUT}V_{DD}}{2I_{OUT-SAT-D}} = \frac{50 fF \cdot 2.5V}{100 \mu A} = 1.25 ns$$

$\frac{3}{4} V_{DD}$ is the average value of $V_{OUT}$

Approximate the NMOS device curve by a straight line from $(0,0)$ to $(I_{OUT-SAT-D}, \frac{3}{4} V_{DD})$.

Interpret the straight line as a resistor with

$$\text{slope} = \frac{1}{R} = \frac{3}{4} V_{DD}/I_{SAT}$$
Switched Equivalent Resistance Values

The resistor values depend on the properties of silicon, geometrical layout, design style and technology node.

- n-type silicon has a carrier mobility that is 2 to 3 times higher than p-type.
- The resistance is inversely proportional to the gate width/length in the geometrical layout.
- Design styles may restrict all NMOS and PMOS to be of a predetermined fixed size.
- The current per unit width of the gate increases nearly inversely with the linewidth.

*For convenience in EE 42 we assume*  
\[ R_D = R_U = 10 \, k\Omega \text{ for } V_{DD} = 5V \text{ and} \]  
\[ R_D = R_U = 10 \, k\Omega \text{ for } V_{DD} = 5V \]

Inverter Propagation Delay

**Discharge (pull-down)**

\[ \Delta t = 0.69R_D C_{OUT} = 0.69(10k\Omega)(50fF) = 345 \text{ ps} \]

**Discharge (pull-up)**

\[ \Delta t = 0.69R_U C_{OUT} = 0.69(10k\Omega)(50fF) = 345 \text{ ps} \]
CMOS Logic Gate

NMOS and PMOS use the same set of input signals

PMOS only in pull-up
PMOS conduct when input is low
PMOS do not conduct when A + (BC)

NMOS only in pull-down
NMOS conduct when input is high.
NMOS conduct for A + (BC)

Logic is Complementary and produces F = A + (BC)

CMOS Logic Gate: Example Inputs

A = 0
B = 0
C = 0

PMOS all conduct
Output is High

= V_{DD}

NMOS do not conduct

Logic is Complementary and produces F = 1
CMOS Logic Gate: Example Inputs

A = 0
B = 1
C = 1

PMOS A conducts; B and C Open
Output is High

PMOS A conducts; B and C Open
Output is High

NMOS B and C conduct; A open

Logic is Complementary and produces F = 0

Switched Equivalent Resistance Network

Switches close when input is low.

Switches close when input is high.
Logic Gate Propagation Delay: Initial State

The initial state depends on the old (previous) inputs.

The equivalent resistance of the pull-down or pull-up network for the transient phase depends on the new (present) input state.

Example: A=0, B=0, C=0 for a long time.

These inputs provided a path to $V_{DD}$ for a long time and the capacitor has precharged up to $V_{DD} = 5V$.

Logic Gate Propagation Delay: Transient

At $t=0$, B and C switch from low to high ($V_{DD}$) and A remains low.

This breaks the path from $V_{OUT}$ to $V_{DD}$

And opens a path from $V_{OUT}$ to GND

$C_{OUT}$ discharges through the pull-down resistance of gates B and C in series.

$$\Delta t = 0.69(R_{DB} + R_{DC})C_{OUT} = 0.69(20k\Omega)(50fF) = 690 \text{ ps}$$

The propagation delay is two times longer than that for the inverter!
Logic Gate: Worst Case Scenarios

What combination of previous and present logic inputs will make the Pull-Up the fastest?

What combination of previous and present logic inputs will make the Pull-Up the slowest?

What combination of previous and present logic inputs will make the Pull-Down the fastest?

What combination of previous and present logic inputs will make the Pull-Down the slowest?

Fastest overall?

Slowest overall?

Logic Gate Cascade

To avoid large resistance due to many gates in series, logic functions with 4 or more inputs are usually made from cascading two or more 2-4 input blocks.

The four independent input are A1, B1, A2 and C2.

A2 high discharges gate 2 without even waiting for the output of gate 1.

C2 high and A2 low makes gate 2 wait for Gate 1 output.