Lecture 19: Logic Transients

A) Quiz
B) Worst Case CMOS Delay
C) Delay in CMOS Cascade

Composite Current Plot for the 42S_NMOS Circuit with 200kΩ Load to Ground

Composite I_{OUT} vs. V_{OUT} for CMOS

Output Propagation Delay High to Low (Cont.)

R_D = \frac{3}{4} \frac{V_{DD}}{I_{SAT}} has a Physical Interpretation

\frac{V_{OUT}(0) = 5V}{C_{OUT} = 50 \mu F}\quad I_{OUT-SAT-D} = 100 \mu A

\frac{V_{IN} = 5}{I_{OUT}(\mu A)}\quad I_{OUT-SAT-D} = 100 \mu A

\frac{R_{PULL-UP} = \frac{3}{4} V_{DD}}{V_{OUT}(\mu A)}\quad I_{OUT-SAT-D} = 100 \mu A

\frac{V_{OUT}(0) = 5V}{C_{OUT} = 50 \mu F}\quad I_{OUT-SAT-D} = 100 \mu A

\frac{V_{OUT} = V_{OUT-SAT-D}}{V_{IN} = 5V}

\frac{I_{OUT}(\mu A)}{V_{OUT}(\mu A)}\quad I_{OUT-SAT-D} = 100 \mu A

\frac{V_{DD} = 5}{I_{OUT}(\mu A)}\quad I_{OUT-SAT-D} = 100 \mu A

\frac{V_{OUT}(0) = 5V}{C_{OUT} = 50 \mu F}\quad I_{OUT-SAT-D} = 100 \mu A

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\frac{V_{DD} = 5}{I_{OUT}(\mu A)}\quad I_{OUT-SAT-D} = 100 \mu A
Switched Equivalent Resistance Values

The resistor values depend on the properties of silicon, geometrical layout, design style and technology node.

- n-type silicon has a carrier mobility that is 2 to 3 times higher than p-type.
- The resistance is inversely proportional to the gate width/length in the geometrical layout.
- Design styles may restrict all NMOS and PMOS to be of a predetermined fixed size.
- The current per unit width of the gate increases nearly inversely with the linewidth.

For convenience in EE 42 we assume

\[ R_D = R_U = 10 \text{k}\Omega \text{ for } V_{DD} = 5\text{V} \] and

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Inverter Propagation Delay

**Discharge (pull-down)**

\[ \Delta t = 0.69 R_D C_{OUT} = 0.69(10\text{ k}\Omega)(50\text{ fF}) = 345 \text{ ps} \]

**Discharge (pull-up)**

\[ \Delta t = 0.69 R_U C_{OUT} = 0.69(10\text{ k}\Omega)(50\text{ fF}) = 345 \text{ ps} \]

CMOS Logic Gate

NMOS and PMOS are the same set of input signals

- PMOS only in pull-up
- PMOS conduct when input is low
- PMOS do not conduct when \( A + (BC) \)
- NMOS only in pull-down
- NMOS conduct when input is high
- NMOS conduct for \( A + (BC) \)
- Logic is Complementary and produces \( F = A + (BC) \)

CMOS Logic Gate: Example Inputs

- \( A = 0 \)
- \( B = 0 \)
- \( C = 0 \)
- PMOS all conduct
- Output is High
- \( V_{OUT} = V_{DD} \)
- NMOS do not conduct
- Logic is Complementary and produces \( F = 1 \)

Switched Equivalent Resistance Network

- PMOS A conducts; B and C Open
- Output is High
- \( V_{OUT} = 0 \)
- NMOS B and C conduct; A open
- Logic is Complementary and produces \( F = 0 \)

Switches close when input is low.

Switches close when input is high.
Logic Gate Propagation Delay: Initial State

The initial state depends on the old (previous) inputs.

The equivalent resistance of the pull-down or pull-up network for the transient phase depends on the new (present) input state.

Example: A=0, B=0, C=0 for a long time.
These inputs provided a path to VDD for a long time and the capacitor has precharged up to $V_{DD} = 5V$.

$C_{OUT} = 50 \text{ fF}$

Logic Gate Propagation Delay: Transient

At $t=0$, B and C switch from low to high ($V_{DD}$) and A remains low.
This breaks the path from $V_{OUT}$ to $V_{DD}$
And opens a path from $V_{OUT}$ to GND
$C_{OUT}$ discharges through the pull-down resistance of gates B and C in series.

$T = 0.69(R_{DB} + R_{DC})C_{OUT} = 0.69(20k\Omega)(50fF) = 690 \text{ ps}$

The propagation delay is two times longer than that for the inverter!

Logic Gate: Worst Case Scenarios

What combination of previous and present logic inputs will make the Pull-Up the fastest?
What combination of previous and present logic inputs will make the Pull-Up the slowest?

Fastest overall?
Slowest overall?

Logic Gate Cascade

To avoid large resistance due to many gates in series, logic functions with 4 or more inputs are usually made from cascading two or more 2-4 input blocks.

The four independent input are A1, B1, A2 and C2.
A2 high discharges gate 2 without even waiting for the output of gate 1.
C2 high and A2 low makes gate 2 wait for Gate 1 output.