EECS 42 Introduction to Electronics for Computer Science

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Lecture # 20 Logic Transients

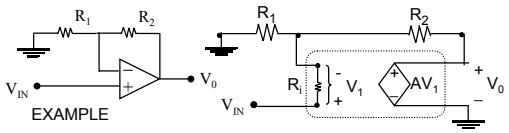
Handout of Monday Lecture.

A) 2nd Midterm Review (Cont.)
B) Intenal Path Propagation Delay
C) Cascade CMOS elements
D) Logic Feedback creates memory

http://inst.EECS.Berkeley.EDU/~ee42/

OP-AMP AND USE OF FEEDBACK

A very high-gain differential amplifier can function in an extremely linear fashion as an operational amplifier by using negative feedback.



Circuit Model

Negative feedback ⇒ **Stabilizes** the output

We can show that that for $A \to \infty$ and $R_i \to \infty$,

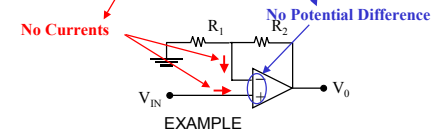
$$V_0 \cong V_{IN} \cdot \frac{R_1 + R_2}{R_1}$$

Stable, finite, and independent of the properties of the OP AMP !

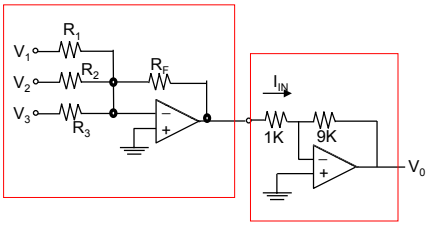
IDEAL OP-AMPS ANALYSIS TECHNIQUE

Assumption 1: The potential between the op-amp input terminals, $v_{(+)} - v_{(-)}$, equals zero.

Assumption 2: The currents flowing into the op-amp's two input terminals both equal zero.



CASCADE OP-AMP CIRCUITS



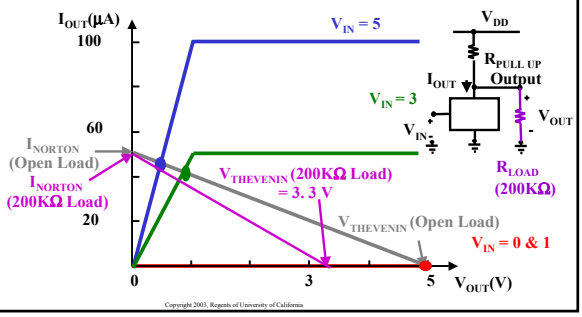
How do you get started on finding V_O?

Hint: Identify Stages

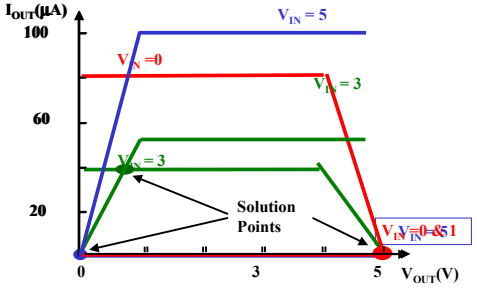
Hint: I_{IN} does not affect V_{O1}

See the further examples of op-amp circuits in the reader

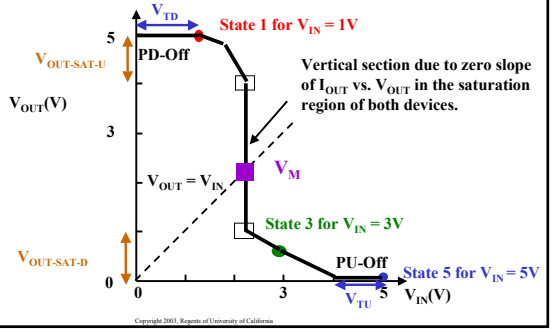
Composite Current Plot for the 42S_NMOS Circuit with 200kΩ Load to Ground



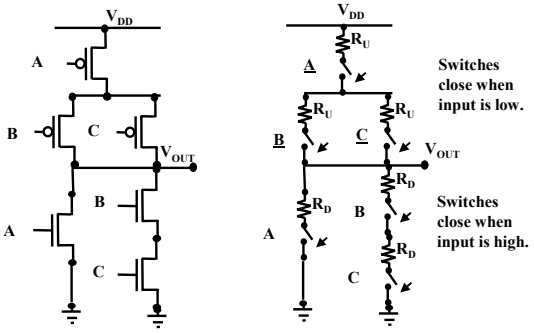
Composite I_{OUT} vs. V_{OUT} to Find Points That Satisfies Both Devices for Each V_{IN}



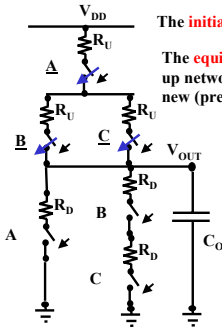
Voltage Transfer Function for the Complementary Logic Circuit



Switched Equivalent Resistance Network



Logic Gate Propagation Delay: Initial State



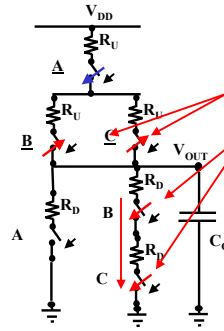
The initial state depends on the old (previous) inputs.

The equivalent resistance of the pull-down or pull-up network for the transient phase depends on the new (present) input state.

Example: A=0, B=0, C=0 for a long time.

These inputs provided a path to V_{DD} for a long time and the capacitor has precharged up to V_{DD} = 5V.

Logic Gate Propagation Delay: Transient



At t=0, B and C switch from low to high (V_{DD}) and A remains low.

This breaks the path from V_{OUT} to V_{DD}

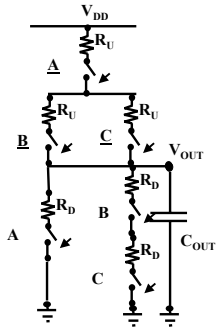
And opens a path from V_{OUT} to GND

C_{OUT} discharges through the pull-down resistance of gates B and C in series.

$\Delta t = 0.69(R_{DB}+R_{DC})C_{OUT}$
$= 0.69(20k\Omega)(50fF) = 690$ ps

The propagation delay is two times longer than that for the inverter!

Logic Gate: Worst Case Scenarios



What combination of previous and present logic inputs will make the Pull-Up the fastest?

What combination of previous and present logic inputs will make the Pull-Up the slowest?

What combination of previous and present logic inputs will make the Pull-Down the fastest?

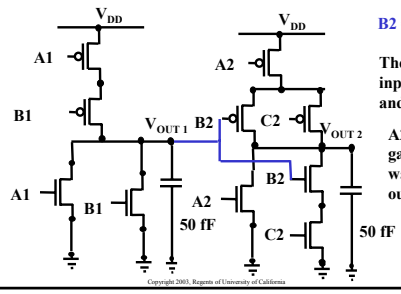
What combination of previous and present logic inputs will make the Pull-Down the slowest?

Fastest overall?

Slowest overall?

Logic Gate Cascade

To avoid large resistance due to many gates in series, logic functions with 4 or more inputs are usually made from cascading two or more 2-4 input blocks.



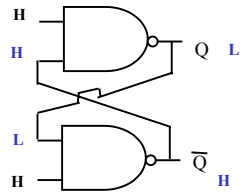
$B2 = V_{OUT\,1}$

The four independent input are A1, B1, A2 and C2.

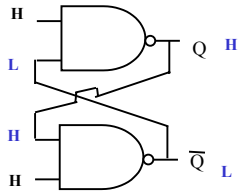
A2 high discharges gate 2 without even waiting for the output of gate 1.

C2 high and A2 low makes gate 2 wait for Gate 1 output

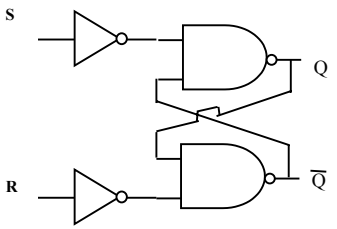
Feedback Can Provide Memory



Example of the Opposite State

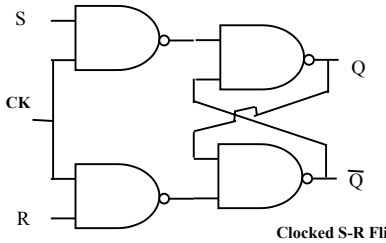


Adding Memory Controls



Set-Reset Flip-Flop

Adding a Clock



Clocked S-R Flip-Flop