EECS 42 Introduction Digital Electronics

Andrew R. Neureuther

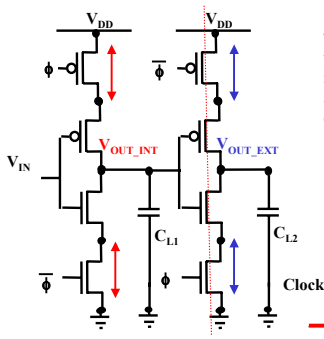
Lecture # 22 Latches and Pipelining

Handout of This Lecture.

A) Timing Diagram for a Clocked Latch
B) Pipelining
C) Latency and Throughput

http://inst.EECS.Berkeley.EDU/~ee42/

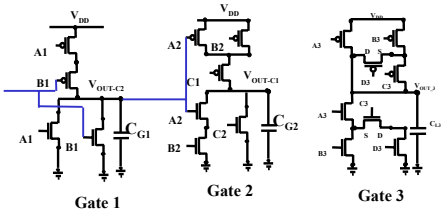
Latch Work Best In Pairs



The first stage operates while the clock is low and inverts and amplifies the arriving signal and charges or discharges C_{L1}.

The second stage operates while the clock is high and inverts the signal on C_{L1} to charge or discharge C_{L2} and downstream logic gate inputs.

Example of Circuits to Integrate with Latches

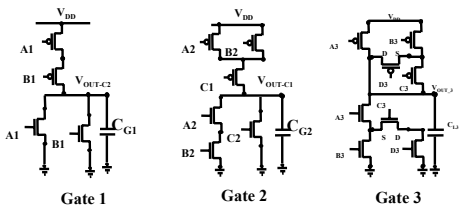


$\tau_{PD\_CASCADE} = \tau_{PD\_1} + \tau_{PD\_2}$

$\tau_{HL} = 3\tau_{INV}$

$\tau_{LH} = 3\tau_{INV}$

Logic Worst Case Delays

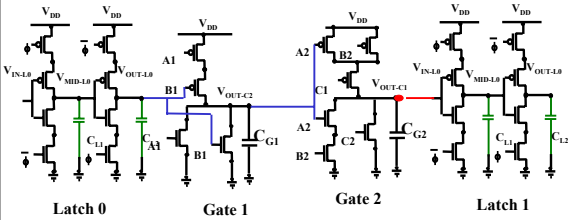


Gate 1: $\tau_{LH} = 2\tau_{INV}$

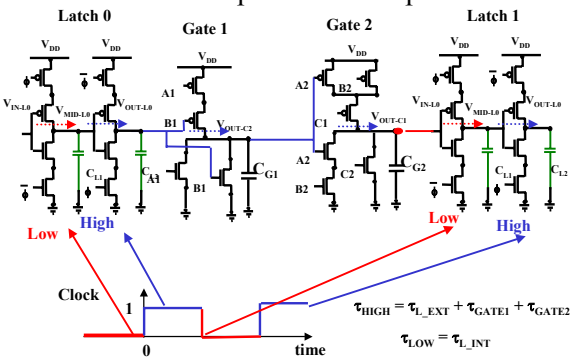
Gate 2: $\tau_{HL} = 2\tau_{INV}$, $\tau_{LH} = 2\tau_{INV}$

Gate 3: $\tau_{HL} = 3\tau_{INV}$, $\tau_{LH} = 3\tau_{INV}$

Latch Implementation: Lumped



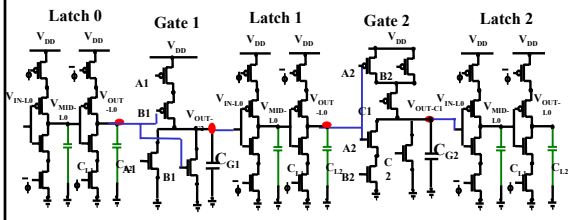
Latch Operation: Lumped



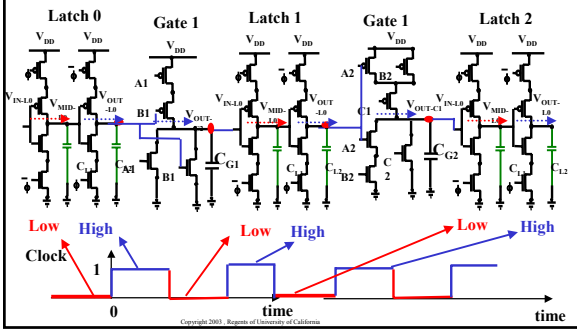
$\tau_{HIGH} = \tau_{L\_EXT} + \tau_{GATE1} + \tau_{GATE2}$

$\tau_{LOW} = \tau_{L\_INT}$

Latch Implementation: Pipelined



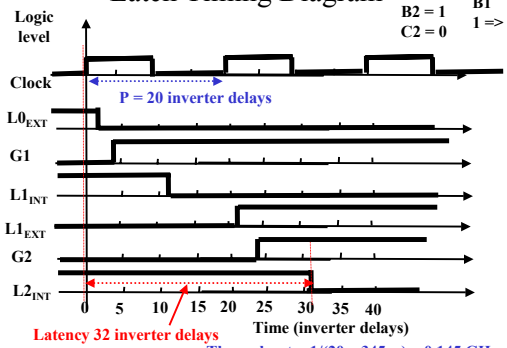
Latch Operation: Pipelined



Latch Timing Diagram

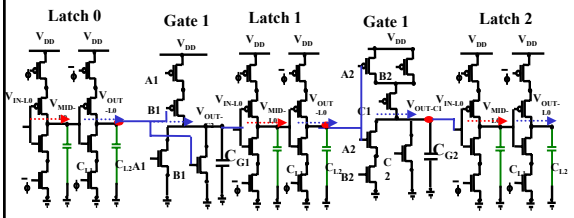
A1 = 0
B2 = 1
C2 = 0

B1
1 => 0



Throughput = 1/(20 x 345ps) = 0.145 GHz

Clock Optimization: Pipelined



$\tau_{HIGH} = \tau_{L\_EXT} + \max(\tau_{GATE1}, \tau_{GATE2})$

$\tau_{LOW} = \tau_{L\_INT}$

Latency and Throughput

Latency L is the delay between the rising edge of the clock on L0 and the data being valid internally in the last latch.

$$L_{LUMPED} = \tau_{L\_EXT} + \tau_{GATE1} + \tau_{GATE2} + \tau_{L\_INT}$$
$$= 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} = 8\tau_{INV}$$

$$L_{PIPLINED} = \tau_{L\_EXT} + \tau_{GATE1} + \tau_{L\_INT} + \tau_{L\_EXT} + \tau_{GATE2} + \tau_{L\_INT}$$
$$= 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} = 12\tau_{INV}$$

Throughput T is the bits per second through the latches and is the maximum clock frequency.

$$P_{LUMPED} = \tau_{L\_EXT} + \tau_{GATE1} + \tau_{GATE2} + \tau_{L\_INT}$$
$$= 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} = 8\tau_{INV}$$

$F_{LUMPED} = 1/8(345ps) = 0.36$ GHz

$$P_{PIPELINED} = \tau_{L\_EXT} + MAX(\tau_{GATE1}, \tau_{GATE2}) + \tau_{L\_INT}$$
$$= 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} = 6\tau_{INV}$$

$F_{PIPLINED} = 1/6(345ps) = 0.48$ GHz

Another Example