

EECS 42 Intro. Digital Electronics Fall 2003 Lecture 24: 11/25/03 A.R. Neureuther
Version Date 11/18/03

EECS 42 Introduction Digital Electronics

Lecture # 24 Current Flow in Silicon and N-MOS Devices

Physics of current flow, resistance, resistivity

- A) Charge transport in a sheet and velocity saturation
- B) N-MOS Device Structure and Voltage Control
- C) N-MOS I vs. V at low and high drain voltage

Reading: Schwarz and Oldham, pp. 518-526

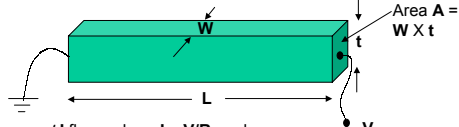
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Physics of Current Flow, Resistance, Resistivity

A voltage V applied across the length L of a homogeneous material produces an electric field E where $E = V/L$.



A current I flows where $I = V/R$ and

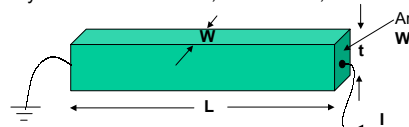
The resistance R is given by the resistor formula $R = \rho L/A$ in which the resistivity, ρ , is inversely proportional to the concentration of free carriers, N , and the mobility of those carriers, μ . (μ is often defined by: |drift velocity| = $\mu E = \mu V/L$)

In fact $\rho = 1/\sigma$, where the conductivity, σ , is defined by $q \mu N$, in which q is the electronic charge ($q = 1.6 \times 10^{-19}$ Coulomb).

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Physics of Current Flow, Resistance, Resistivity



$E = V/L$.
 $I = V/R$
 $R = \rho L/A = (1/q \mu N) L/W t = (L/W) / \mu(q N t)$

Carrier mobility
Carriers per unit volume

But $q N t$ has the dimensions of charge per unit area and represents the charge per unit area in a film of thickness t when the film has N carriers/cm³ and is t units thick. Thus we call $q N t$ the "Q" and

$R = (L/W) / \mu Q = L/W R_{\square}$

Where R_{\square} is the resistance of a "square" of the film. Clearly if L is four times W , then $R = 4 R_{\square}$.

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Resistance of Silicon Films (at low E fields)

at low fields $\sigma = q N \mu$ where $N = n$ or p and $\mu = \mu_n$ or μ_p

So $\sigma = q n \mu_n$ for electrons in n-type Si
and $\sigma = q p \mu_p$ for holes in p-type Si

In other words $R_{\square} = 1/\mu_n(q N_D t) = 1/\mu_n(Q_D)$ in N-type Silicon

Where $(N_D t)$ is the number of donors implanted per unit area, and multiplying by q , we have the donor charge implanted per unit area. (μ_n is the mobility of the electrons).

Similarly $R_{\square} = 1/\mu_p(q N_A t) = 1/\mu_p(Q_A)$ in P-type Silicon

Where $(N_A t)$ is the number of acceptors implanted per unit area, and multiplying by q , we have the acceptor charge implanted per unit area.

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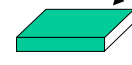
Silicon Resistor

Example: 1 μm thick n-type silicon layer which was implanted with 10^{12} donors cm^{-2} . (Thus $N_D = 10^{12} / 10^{-4} = 10^{16} \text{ cm}^{-3}$)

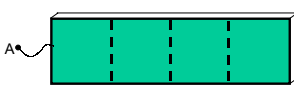
$\sigma = q n \mu_n = (1.6 \times 10^{-19} \text{ C}) (10^{16} \text{ cm}^{-3}) (1000 \text{ cm}^2/\text{Vsec}) = 1.6 \text{ S/cm}$

$\rho = 1/\sigma = 0.625 \Omega \text{ cm}$

Sheet resistivity, R_{\square} given by:
 $R_{\square} = [1/(\sigma t)] = 6.25 \text{ K}\Omega/\text{square}$



But this can be obtained directly from the implant "Q" of $1.6 \times 10^{-19} \times 10^{12} = 1.6 \times 10^{-7}$ thus
 $R_{\square} = [1/(Q \mu)] = 6.25 \text{ K}\Omega/\text{square}$



$R_{AB} = ?$
 $R_{AB} = 4 \times 6.25 = 25 \text{ K}\Omega$

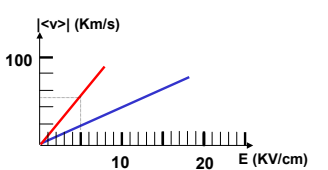
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Charge Transport in Silicon

At low electric fields, the average speed of carriers is proportional to the field with proportionality constant μ ; In fact drift velocity = $\mu_p E$ for holes = $-\mu_n E$ for electrons :

Example: $\mu_n = 1000 \text{ cm}^2/\text{V-sec}$, (or $10 \text{ Km}^2/\text{KV-sec}$)
 $\mu_p = 500 \text{ cm}^2/\text{V-sec}$



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Charge Transport in Silicon

But at **high electric fields**, the average speed of carriers is **NOT** proportional to the field; that is the mobility concept fails. In fact velocity saturates at 10^7 cm/sec = 100 km/sec for both electrons and holes:

This saturation is observable directly in the "resistance" of a silicon resistor at high fields ($10\text{KV/cm} = 1\text{V}/\mu\text{m}$)

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THE "CHARGE CONTROL DEVICE" OR HOW TO MAKE A SMART SWITCH

Concept:
Apply positive voltage to gate with respect to semiconductor. This will induce +Q on gate, -Q on surface of semiconductor. Resistance between D and S will drop.

Thus, we can control current from D to S.

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MOS TRANSISTOR STRUCTURE DEVICE IN CROSS-SECTION

"Metal" "Oxide" "Semiconductor"

- In the absence of gate voltage, no current can flow between S and D.
- Above a certain gate to source voltage V_T (the "threshold"), electrons are induced at the surface beneath the oxide. (Think of it as a capacitor.)
- These electrons can carry current between S and D if a voltage is applied.

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CHARGE-CONTROL EXPERIMENT – "THE FIELD EFFECT"

Above some "threshold" voltage V_T , the number of electrons per square cm under the gate is proportional to $V_{GS} - V_T$, i.e., the charge Q_N is proportional to $V_{GS} - V_T$.

These charge carriers can carry current from D to S, so we can make low resistance (R_{DS}) by making $V_{GS} - V_T$ very large

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I-V CHARACTERISTICS IN THE LOW V_{DS} REGIME

Consider first gate current and drain current versus GATE voltage

The gate is insulated, so there can never be any gate current.

always zero!

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I-V CHARACTERISTICS IN THE LOW V_{DS} REGIME

Consider i_{DS} , the current from D to S:

Below "threshold" no charge, so no conduction. ($V_{GS} < V_T$)
Above threshold ($V_{GS} > V_T$), Q appears so drain to source conduction is possible
Very low resistance (R_{DS}) for increasing gate voltage ($V_{GS} \gg V_T$)

We have a controlled switch !

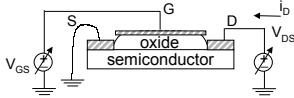
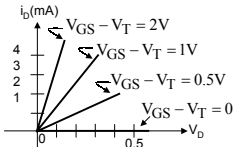
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I-V CHARACTERISTICS IN LOW V_{DS} REGIME (cont.)

The drain current is a linear function of drain voltage at low drain voltages

MOS is just a (linear) controlled resistor in the low V_{DS} regime with the drain-to-source resistance depending on how much voltage is applied to the gate (compared to threshold).

Example of a device characteristic for low V_{DS}



CLEARLY A "CONTROLLED SWITCH"

N-MOS I-V Characteristics

At low V_{DS} we have:

$$I_D = \frac{W}{L} \frac{V_{DS}}{R_{\square}} = \frac{W}{L} \mu_n C_{ox} (V_{GS} - V_T) \cdot V_{DS}$$

[Note that this also follows from our previous analysis where we had :

$$I = q W t \mu_n n v/L = Q_n \mu_n W/L V$$

because $Q = C_{ox} (V_{GS} - V_T)$]

And of course already know what happens to the I-V characteristics of short-channel MOS devices at higher values of V_{DS} : We know that the curves "bend over" because of velocity saturation.

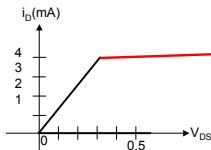
What about Larger Drain-Source Voltages -- What Happens?

In digital circuits we always use the "shortest" gate length devices possible for reasons of speed. Fortunately this makes the answer to the question above very simple:

For such short-channel devices the drain current saturates because the carriers can only move at a limited speed

We can approximate the I-V characteristics as two straight lines:

- the linear "resistance" region at low V_{DS} and
- the velocity saturation region (almost horizontal) at larger V_{DS} .



Saturation Current NMOS Model

Current I_{OUT} only flows when V_{IN} is larger than the threshold value V_{TD} and the current is proportional to V_{OUT} up to $V_{OUT-SAT-D}$ where it reaches the saturation current

$$I_{OUT-SAT-D} = k_D (V_{IN} - V_{TD}) V_{OUT-SAT-D}$$

Note that we have added an extra parameter to distinguish between threshold (V_{TD}) and saturation ($V_{OUT-SAT-D}$).

Example:

$$k_D = 25 \mu A/V^2 \quad \text{Use these values in the homework.}$$

$$V_{TD} = 1V$$

$$V_{OUT-SAT-D} = 1V$$

$$I_{OUT-SAT-PD} = 25 \frac{\mu A}{V^2} (3V - 1V) 1V = 50 \mu A$$

