

## Review for the Final Exam

**Likely 7 Problems** \* Possible Bonus = 2/3 best +1/3 worst

**Midterm Bonus = 2/3 best +1/3 worst**

**Transients\***

**Logic Functions and Timing Diagrams**

**Circuit Analysis with dependent Sources**

**Op-Amps\***

**Load Line and Static Analysis of Logic Gates**

**CMOS Logic Functions, Delay, Latches**

**Diode Circuit Analysis, Voltage Controlled R**

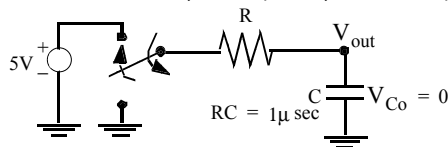
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### PULSE: Output is Rising exponential then Falling exponential

#### Lecture 7

Example: Switch rises at  $t=0$ , falls at  $t = 0.1, 1$  or  $10\mu\text{sec}$  (Do  $1\mu\text{sec}$  case)



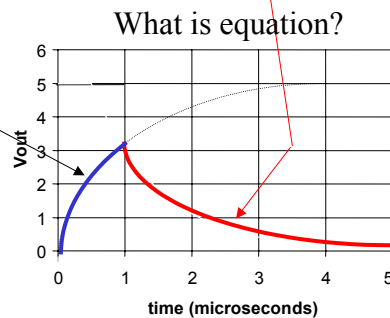
Solution: for  $RC = 1\mu\text{sec}$ :  
during the first rise  $V$  obeys:

$$V = 5 \left[ 1 - e^{-\frac{t}{10^{-6}}} \right]$$

Thus at  $t = 1\mu\text{sec}$ , rising voltage reaches

$$5 \left[ 1 - e^{-1} \right] = 3.16\text{V}$$

Now starting at  $1\mu\text{sec}$  we are discharging the capacitor so the form is a falling exponential with initial value  $3.16\text{V}$ :

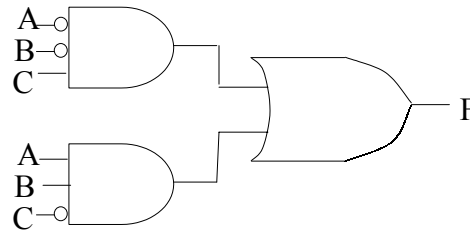


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### How to Combine Gate to Produce a Desired Logic Function? (More basic Logical Synthesis)

Example:

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0



$$F = \overline{A} \overline{B} C + A B \overline{C}$$

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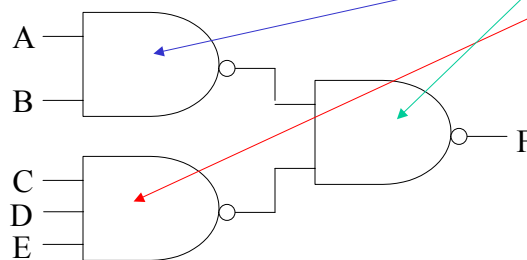
### Logical Synthesis Guided by DeMorgan's Theorem

DeMorgan's Theorem :

$$A + B + C = \overline{[\overline{A} \overline{B} \overline{C}]} \quad \text{or} \quad \overline{A} + \overline{B} + \overline{C} = \overline{[A B C]}$$

Example of Using DeMorgan's Theorem:

$$F = A \bullet B + C \bullet D \bullet E = \overline{[\overline{A B} \bullet \overline{C D E}]}$$

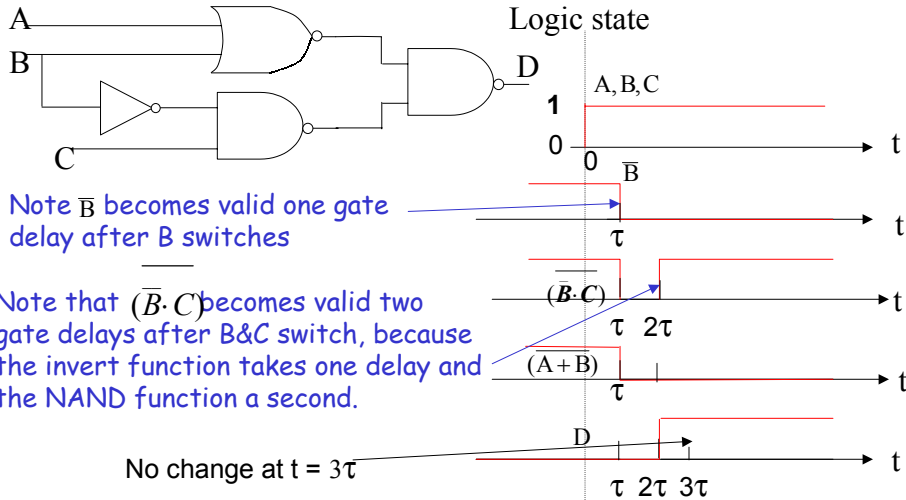


Thus any sum of products expression can be immediately synthesized from NAND gates alone

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### TIMING DIAGRAMS

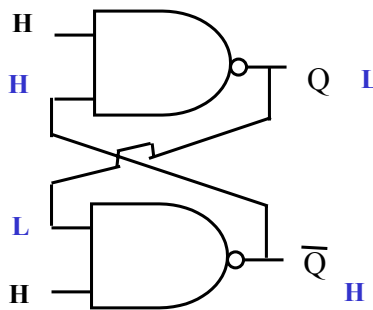
Show transitions of variables vs time



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### Feedback Can Provide Memory

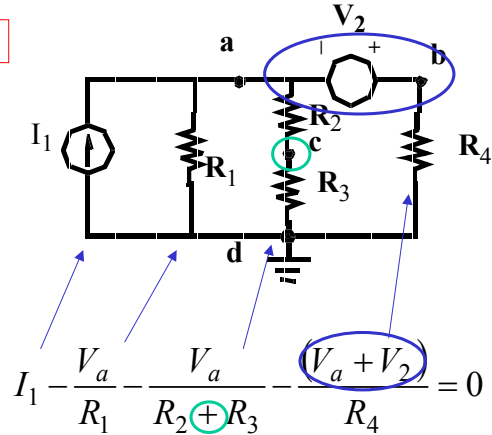
Lecture 19



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**EXAMPLE WITH BOTH SPECIAL CASES**

Lecture 8



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**The 4 Basic Linear Dependent Sources**

Lecture 13

Constant of proportionality

Parameter being sensed

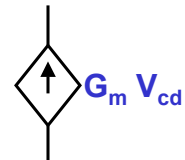
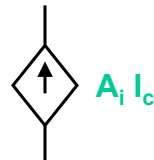
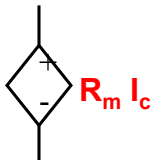
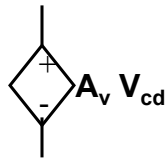
Output

Voltage-controlled voltage source ...  $V = A_v V_{cd}$

Current-controlled voltage source ...  $V = R_m I_c$

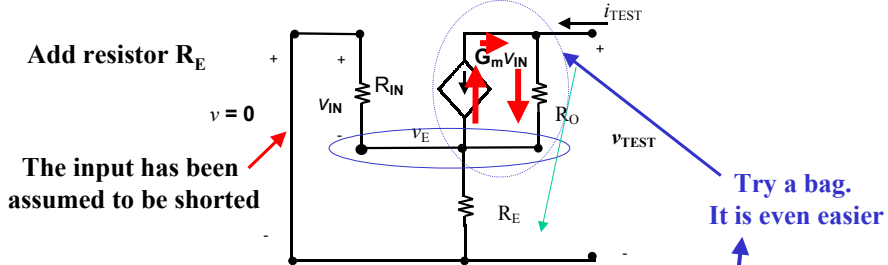
Current-controlled current source ...  $I = A_i I_c$

Voltage-controlled current source ...  $I = G_m V_{cd}$



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**EXAMPLE CIRCUIT: INCREASED OUTPUT RESISTANCE**



Add resistor  $R_E$

The input has been assumed to be shorted  $v = 0$

Analysis: apply  $i_{TEST}$  and evaluate  $v_{TEST}$

Unknowns:  $i_{TEST}$ ,  $v_{TEST}$ ,  $v_{IN}$ ,  $v_E$

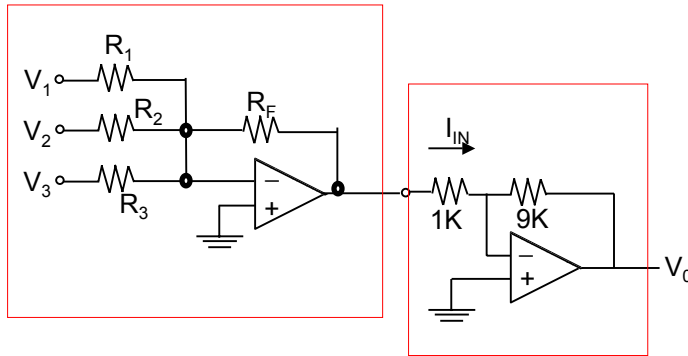
Need 3 equations to find the ratio of  $i_{TEST} / v_{TEST}$

$v_{IN} = -v_E$  and is **not zero!**  
 KCL at  $v_E$   
 KVL at  $v_{OUT}$

Intuitive Explanation:  $G_m V_{IN}$  burps current which has to also go through  $R_O$ . This raises  $v_{TEST}$  and the output impedance  $v_{TEST} / i_{TEST}$

Finish this in the homework

**CASCADE OP-AMP CIRCUITS**



How do you get started on finding  $V_0$ ?

Hint: Identify Stages

Hint:  $I_{IN}$  does not affect  $V_{O1}$

See the further examples of op-amp circuits in the reader

### Saturation Current NMOS Model

Current  $I_{OUT}$  only flows when  $V_{IN}$  is larger than the threshold value  $V_{TD}$  and the current is proportional to  $V_{OUT}$  up to  $V_{OUT-SAT-D}$  where it reaches the saturation current

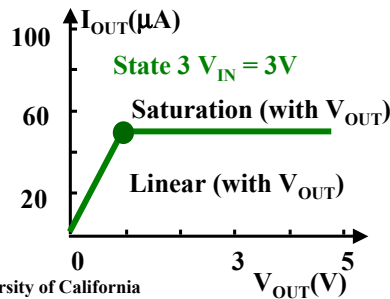
$$I_{OUT-SAT-D} = k_D (V_{IN} - V_{TD}) V_{OUT-SAT-D}$$

Note that we have added an extra parameter to distinguish between threshold ( $V_{TD}$ ) and saturation ( $V_{OUT-SAT-D}$ ).

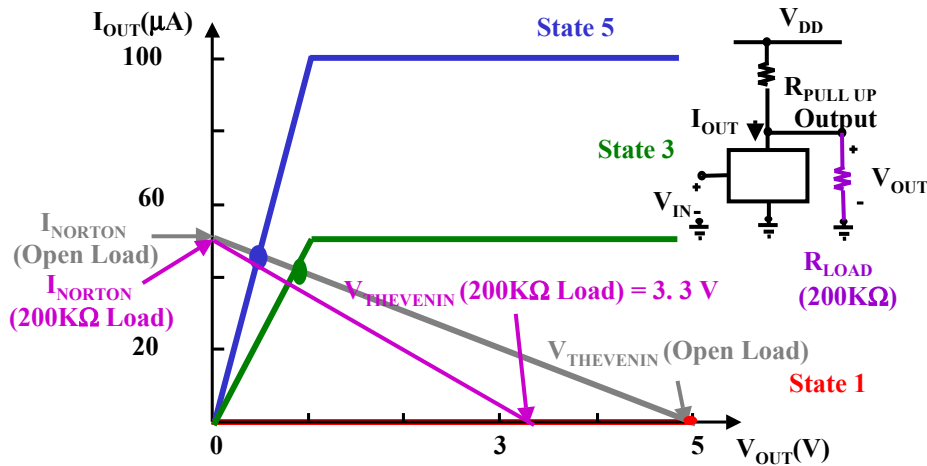
Example:

$k_D = 25 \mu A/V^2$     Use these values in the homework.  
 $V_{TD} = 1V$   
 $V_{OUT-SAT-D} = 1V$

$$I_{OUT-SAT-PD} = 25 \frac{\mu A}{V^2} (3V - 1V) 1V = 50 \mu A$$

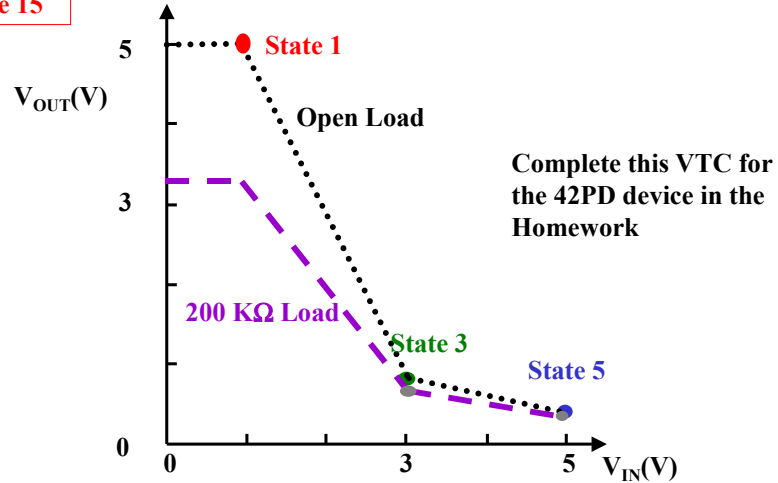


### Composite Current Plot for the 42PD Circuit with 200kΩ Load to Ground



## Voltage Transfer Function for the 42PD Logic Circuit w/wo Load

Lecture 15

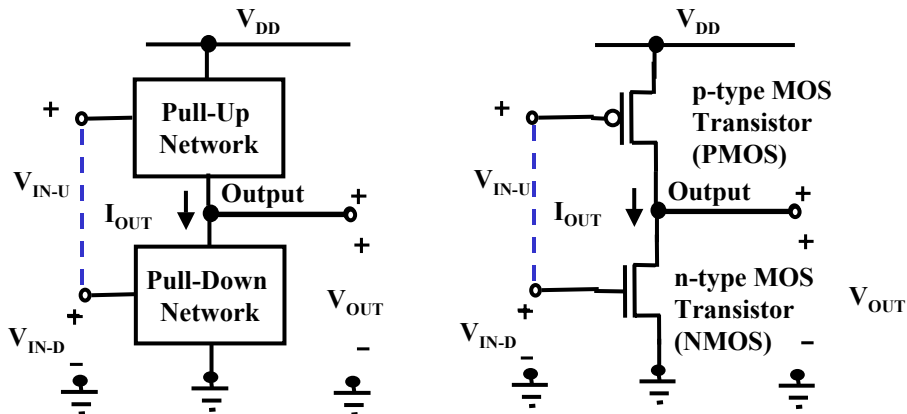


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Lecture 17

## Transistor Inverter Example

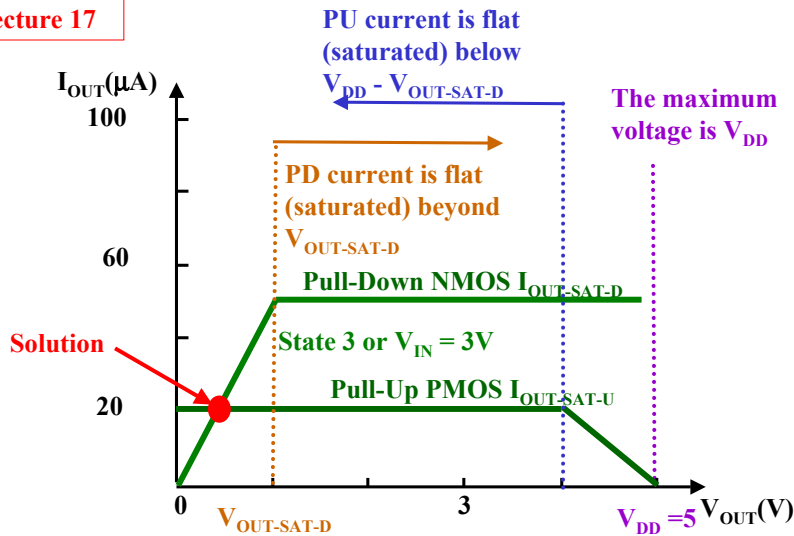
It may be simpler to just think of PMOS and NMOS transistors instead of a general 3 terminal pull-up or pull-down devices or networks.



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## Composite $I_{OUT}$ vs. $V_{OUT}$ for CMOS

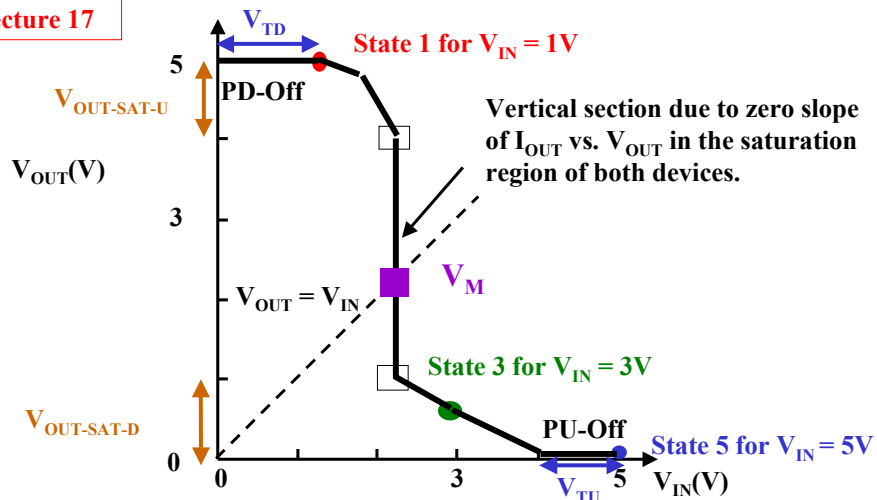
Lecture 17



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## Voltage Transfer Function for the Complementary Logic Circuit

Lecture 17

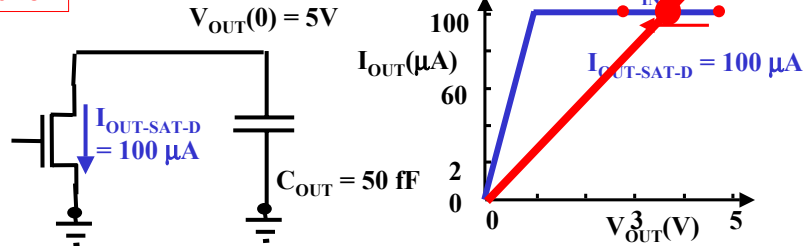


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### $\frac{3}{4} V_{DD}/I_{SAT}$ Physical Interpretation

Lecture 18



$\frac{3}{4} V_{DD}$  is the average value of  $V_{OUT}$

Approximate the NMOS device curve by a straight line from (0,0) to ( $I_{OUT-SAT-D}, \frac{3}{4} V_{DD}$ ).

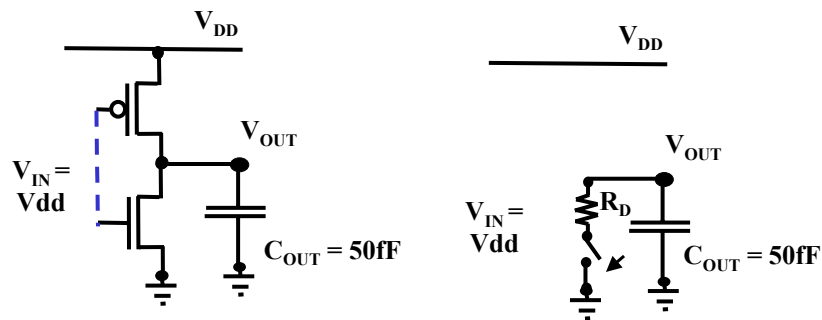
Interpret the straight line as a resistor with

$$\text{slope} = 1/R = \frac{3}{4} V_{DD}/I_{SAT}$$

Lecture 18

### Inverter Propagation Delay

Discharge (pull-down)



$$\Delta t = 0.69R_D C_{OUT} = 0.69(10k\Omega)(50fF) = 345 \text{ ps}$$

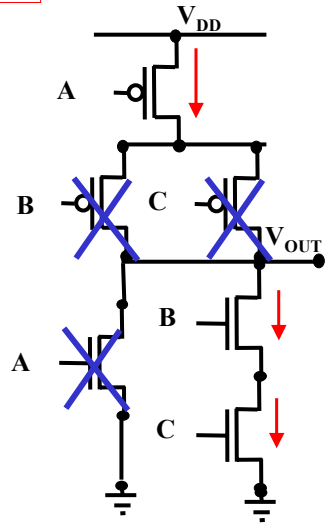
Discharge (pull-up)

$$\Delta t = 0.69R_U C_{OUT} = 0.69(10k\Omega)(50fF) = 345 \text{ ps}$$

Lecture 18

### CMOS Logic Gate: Example Inputs

A = 0  
B = 1  
C = 1



PMOS A conducts; B and C Open

Output is High

= 0

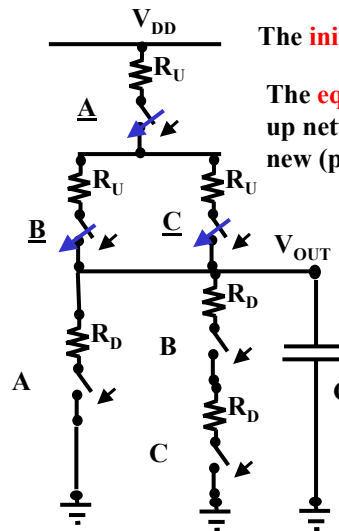
NMOS B and C conduct; A open

Logic is Complementary and produces F = 0

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Lecture 19

### Logic Gate Propagation Delay: Initial State



The **initial state** depends on the old (previous) inputs.

The **equivalent resistance** of the pull-down or pull-up network for the transient phase depends on the new (present) input state.

Example: A=0, B=0, C=0 for a long time.

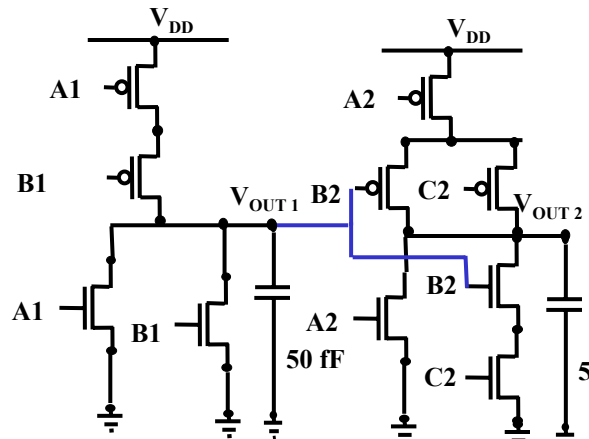
These inputs provided a path to  $V_{DD}$  for a long time and the capacitor has precharged up to  $V_{DD} = 5V$ .

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**Lecture 20**

# Logic Gate Cascade

To avoid large resistance due to many gates in series, logic functions with 4 or more inputs are usually made from cascading two or more 2-4 input blocks.



$B2 = V_{OUT1}$

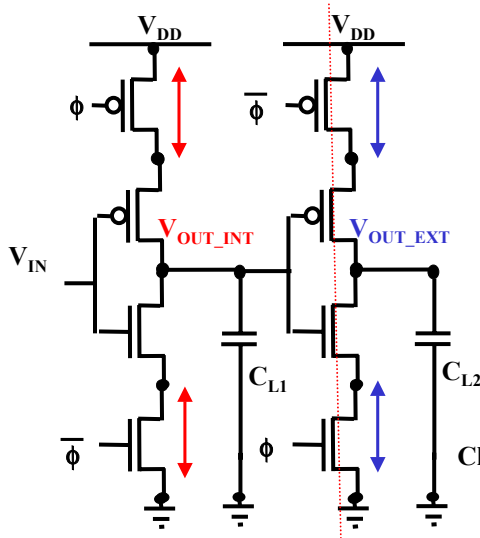
The four independent input are A1, B1, A2 and C2.

A2 high discharges gate 2 without even waiting for the output of gate 1.

C2 high and A2 low makes gate 2 wait for Gate 1 output

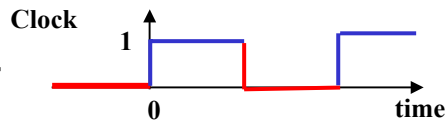
**Lecture 21**

# Latch Work Best In Pairs



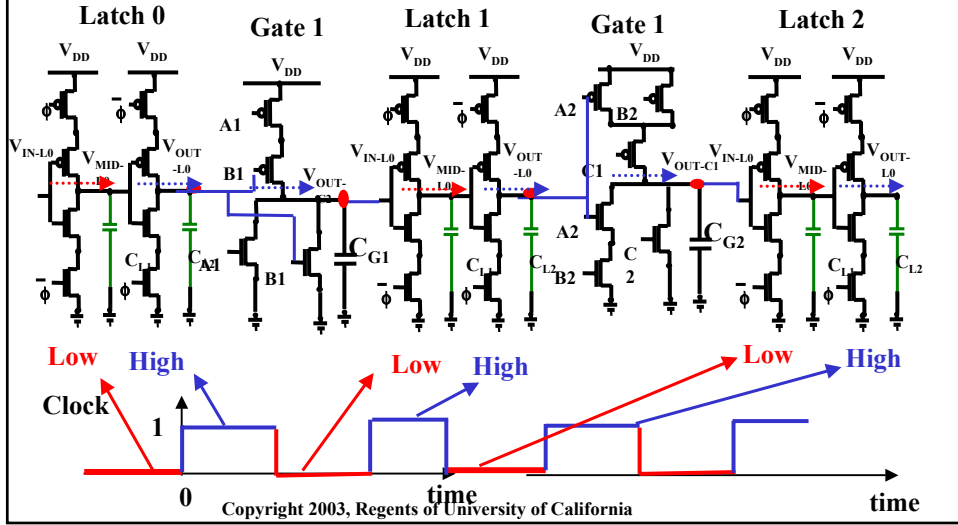
The first stage operates while the clock is low and inverts and amplifies the arriving signal and charges or discharges  $C_{L1}$ .

The second stage operates while the clock is high and inverts the signal on  $C_{L1}$  to charge or discharge  $C_{L2}$  and downstream logic gate inputs.



Lecture 22

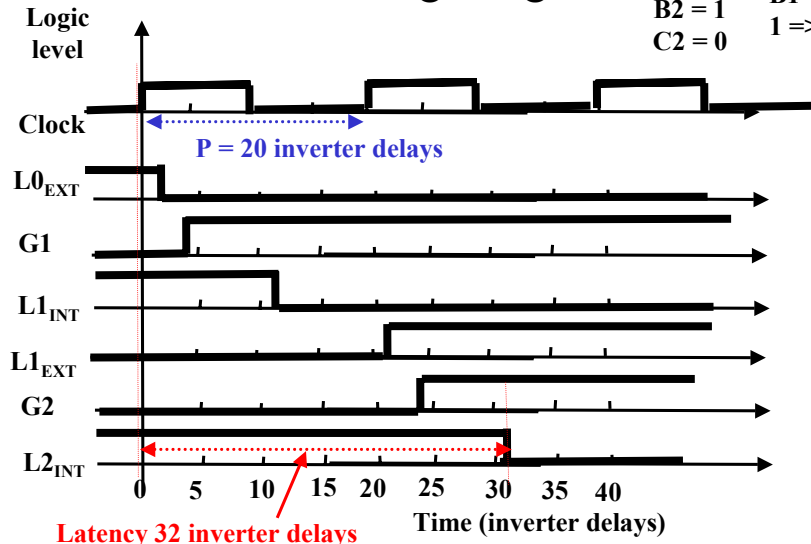
# Latch Operation: Pipelined



Lecture 22

# Latch Timing Diagram

A1 = 0  
B2 = 1  
C2 = 0  
B1 = 1 ⇒ 0



Throughput =  $1/(20 \times 345ps) = 0.145$  GHz

**Lecture 22**

## Latency and Throughput

**Latency L** is the delay between the rising edge of the clock on L0 and the data being valid internally in the last latch.

$$\begin{aligned} L_{\text{LUMPED}} &= \tau_{L\_EXT} + \tau_{\text{GATE1}} + \tau_{\text{GATE2}} + \tau_{L\_INT} \\ &= 2\tau_{\text{INV}} + 2\tau_{\text{INV}} + 2\tau_{\text{INV}} + 2\tau_{\text{INV}} = 8\tau_{\text{INV}} \end{aligned}$$

$$\begin{aligned} L_{\text{PIPELINED}} &= \tau_{L\_EXT} + \tau_{\text{GATE1}} + \tau_{L\_INT} + \tau_{L\_EXT} + \tau_{\text{GATE2}} + \tau_{L\_INT} \\ &= 2\tau_{\text{INV}} + 2\tau_{\text{INV}} + 2\tau_{\text{INV}} + 2\tau_{\text{INV}} + 2\tau_{\text{INV}} + 2\tau_{\text{INV}} = 12\tau_{\text{INV}} \end{aligned}$$

**Throughput T** is the bits per second through the latches and is the maximum clock frequency.

$$\begin{aligned} P_{\text{LUMPED}} &= \tau_{L\_EXT} + \tau_{\text{GATE1}} + \tau_{\text{GATE2}} + \tau_{L\_INT} \\ &= 2\tau_{\text{INV}} + 2\tau_{\text{INV}} + 2\tau_{\text{INV}} + 2\tau_{\text{INV}} = 8\tau_{\text{INV}} \\ F_{\text{LUMPED}} &= 1/8(345\text{ps}) = 0.36 \text{ GHz} \end{aligned}$$

$$\begin{aligned} P_{\text{PIPELINED}} &= \tau_{L\_EXT} + \text{MAX}(\tau_{\text{GATE1}}, \tau_{\text{GATE2}}) + \tau_{L\_INT} \\ &= 2\tau_{\text{INV}} + 2\tau_{\text{INV}} + 2\tau_{\text{INV}} = 6\tau_{\text{INV}} \quad F_{\text{PIPELINED}} = 1/6(345\text{ps}) = 0.48 \text{ GHz} \end{aligned}$$

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**Lecture 25: on blackboard**

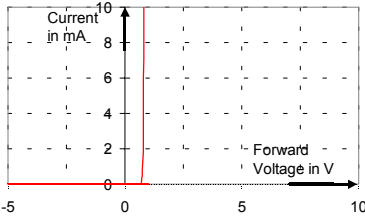
## Limitations of Power Consumption

- The resistive load of NMOS results in D.C. current and hence static power consumption given by the product of current times voltage.
- CMOS avoids this static loss as the pull-up device shuts off the current completely.
- CMOS still suffers a.c. power consumption that is proportional to the switching frequency.
- The energy expended per cycle of in charging and discharging can never be less than  $CV^2$

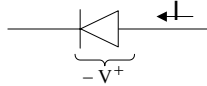
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### DIODE I-V CHARACTERISTICS AND MODELS

The equation  $I = I_0 \exp(qV/kT - 1)$  is graphed below for  $I_0 = 10^{-15}$  A



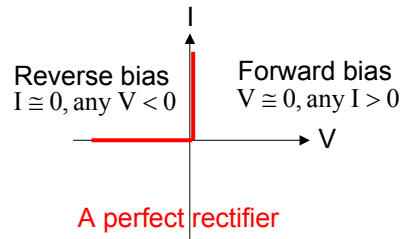
The characteristic is described as a “rectifier” – that is, a device that permits current to pass in only one direction. (The hydraulic analog is a “check valve”.) Hence the symbol:



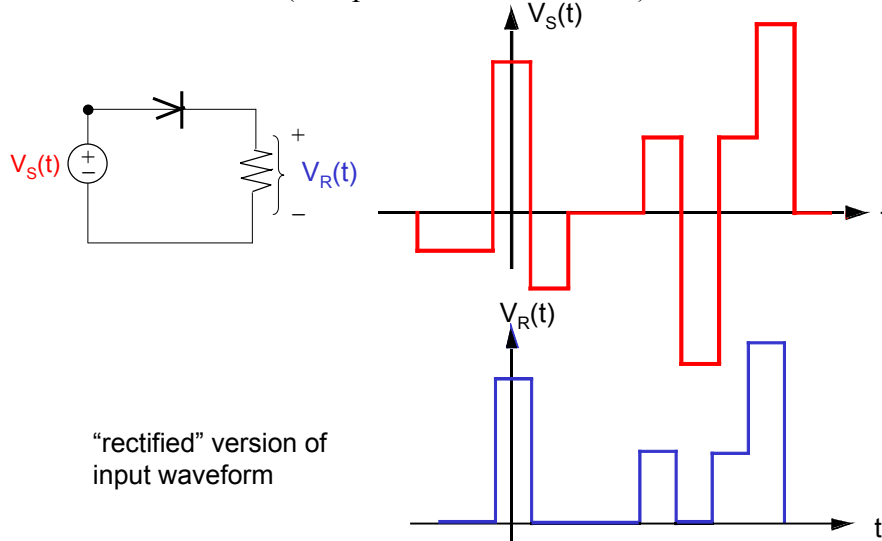
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#### Simple “Perfect Rectifier” Model

If we can ignore the small forward-bias voltage drop of a diode, a simple effective model is the “perfect rectifier,” whose I-V characteristic is given below:



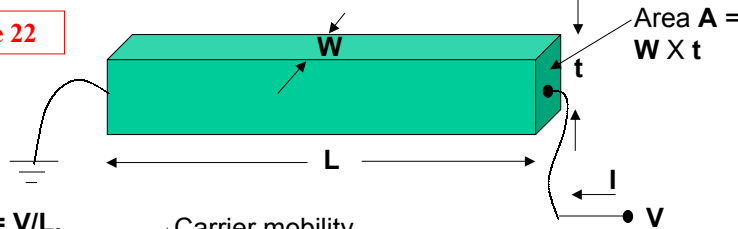
### COOL THINGS A DIODE CAN DO (Use perfect rectifier model)



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## Physics of Current Flow, Resistance, Resistivity

## Lecture 22



$$E = V/L.$$

$$I = V/R$$

$$R = \rho L/A = (1/q \mu N) L/W t = (L/W) / \mu(qNt)$$

But  $q N t$  has the dimensions of charge per unit area and represents the charge per unit area in a film of thickness  $t$  when the film has  $N$  carriers/cm<sup>3</sup> and is  $t$  units thick. Thus we call  $q N t$  the “ $Q$ ” and

$$R = (L/W) / \mu Q = L/W R_{\square}$$

Where  $R_{\square}$  is the resistance of a “square” of the film. Clearly if  $L$  is four times  $W$ , then  $R = 4 R_{\square}$ .

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## Relation of Current to Physical Parameters

$$I_D = \mu_n C_{ox} \left( \frac{W}{L} \right)_n (V_{GS} - V_T) \cdot V_{OUT-SAT-n}$$

Mobility of carriers  $\mu_n$   
 Oxide thickness  $C_{ox}$   
 Geometrical Layout  $(W/L)_n$   
 Excess Gate drive  $(V_{GS} - V_T)$   
 Voltage of scattering velocity limit  $V_{OUT-SAT-n}$

$$\mu_n = 500 (cm^2 / Vs) \quad \mu_p = 150 (cm^2 / Vs)$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{(8.85 \times 10^{-14} F/cm)(3.9)}{6 \times 10^{-7} cm} = 5.75 \times 10^{-7} F/cm^2$$

$$V_{OUT-SAT-n} = E_{Crit} \cdot L = 10^4 (V/cm) \cdot 0.25 \times 10^{-4} cm = 0.25V$$

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