Review for the Final Exam

Likely 7 Problems  * Possible Bonus = 2/3 best +1/3 worst
Midterm Bonus = 2/3 best +1/3 worst

Transients*
Logic Functions and Timing Diagrams
Circuit Analysis with dependent Sources
Op-Amps*
Load Line and Static Analysis of Logic Gates
CMOS Logic Functions, Delay, Latches
Diode Circuit Analysis, Voltage Controlled R

See Web Site under Exams for Coverage, Review Sessions and Office Hours

PULSE: Output is Rising exponential then Falling exponential
Example: Switch rises at t = 0, falls at t = 0.1, 1 or 10 µsec. (Do 1 µsec case)
Now starting at 1 µsec we are discharging the capacitor so the form is a falling exponential with initial value 3.16 V.
Solution: for RC = 1 µsec:
During the first rise V obeys:

\[ V = 5 - (5 - 3.16) e^{t/1} \]

Thus at t = 1 µsec, rising voltage reaches 3.16 V.

What is equation?

Logical Synthesis
Guided by DeMorgan’s Theorem
DeMorgan’s Theorem:

\[ \overline{A + B + C} = \overline{A} \overline{B} \overline{C} \quad \text{or} \quad \overline{A + B + C} = \overline{A B C} \]

Example of Using DeMorgan’s Theorem:

\[ F = A \overline{B} C + \overline{A} B \overline{C} \]

Logical state

Note: becomes valid one gate delay after B switches
Note that becomes valid two gate delays after B & C switch, because the invert function takes one delay and the NAND function a second.
No change at t = 3τ

Feedback Can Provide Memory

Thus any sum of products expression can be immediately synthesized from NAND gates alone

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EXAMPLE WITH BOTH SPECIAL CASES

Lecture 8

EXAMPLE CIRCUIT: INCREASED OUTPUT RESISTANCE

Add resistor \( R_e \)

The input has been assumed to be shorted

Analysis: apply \( i_{\text{TEST}} \) and evaluate \( v_{\text{OUT}} \)

Unknowns: \( i_{\text{TEST}} \), \( v_{\text{OUT}} \)

Need 3 equations to find the ratio of \( V_{\text{TH}} \) to \( V_{\text{SAT}} \) and \( I_{\text{OUT}} \), and \( I_{\text{TEST}} \)

Intuitive Explanation: \( G_m \) burps current which has to also go through \( R_0 \). This raises \( V_{\text{OUT}} \) and the output impedance \( V_{\text{OUT}}/I_{\text{TEST}} \)

Finish this in the homework

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Saturation Current NMOS Model

Current \( I_{\text{OUT}} \) only flows when \( V_{\text{IN}} \) is larger than the threshold value \( V_{\text{TH}} \) and the current is proportional to \( V_{\text{OUT}} \) up to \( V_{\text{OUT,SAT}} \) where it reaches the saturation current

\[
I_{\text{OUT,SAT}} = k_D (V_{\text{IN}} - V_{\text{TH}}) \]

Note that we have added an extra parameter to distinguish between threshold \( V_{\text{TH}} \) and saturation \( V_{\text{OUT,SAT}} \).

Example:

\( k_D = 25 \mu A/V^2 \), \( V_{\text{TH}} = 1V \), \( V_{\text{OUT,SAT}} = 1V \)

\( I_{\text{OUT,SAT}} = 25 \times \left( V_{\text{IN}} - V_{\text{TH}} \right) \times \frac{1V}{50k\Omega} \)

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Composite Current Plot for the 42PD Circuit with 200kΩ Load to Ground

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### Voltage Transfer Function for the 42PD Logic Circuit w/o Load

**Lecture 15**

![Graph showing voltage transfer function](image)

Complete this VTC for the 42PD device in the Homework.

**Lecture 17**

**Transistor Inverter Example**

It may be simpler to just think of PMOS and NMOS transistors instead of a general 3 terminal pull-up or pull-down devices or networks.

**Lecture 17**

**Composite I\textsubscript{OUT} vs. V\textsubscript{OUT} for CMOS**

**Solution**

I\textsubscript{OUT}\textsubscript{SAT-D} = 100 µA

V\textsubscript{OUT}(0) = 5V

C\textsubscript{OUT} = 50 fF

V\textsubscript{OUT}(0) = V\textsubscript{DD}/2

I\textsubscript{OUT}\textsubscript{SAT-D} = 100 µA

Interpret the straight line as a resistor with slope = 1/R = \(\frac{1}{2} V_{DD}/I_{SAT}\)

\(\frac{1}{2} V_{DD}/I_{SAT}\) is the average value of V\textsubscript{OUT}

Approximate the NMOS device curve by a straight line from (0,0) to (I\textsubscript{OUT}\textsubscript{SAT-D}, \(\frac{1}{2} V_{DD}\)).

**Lecture 18**

**Inverter Propagation Delay**

\[ \Delta t = 0.69 R_{DC} C_{OUT} = 0.69(10k \Omega)(50fF) = 345 \text{ ps} \]

Discharge (pull-down)

\[ \Delta t = 0.69 R_{DC} C_{OUT} = 0.69(10k \Omega)(50fF) = 345 \text{ ps} \]
**CMOS Logic Gate: Example Inputs**

- **A = 0, B = 1, C = 1**: PMOS A conducts; B and C open. Logic is complementary and produces $F = 0$.
- **A = 0, B = 1, C = 1**: NMOS B and C conduct; A open.

**Logic Gate Propagation Delay: Initial State**

The initial state depends on the old (previous) inputs. The equivalent resistance of the pull-down or pull-up network for the transient phase depends on the new (present) input state.

**Latch Work Best In Pairs**

The second stage operates while the clock is high and inverts the signal on CL1 to charge or discharge CL2 and downstream logic gate inputs. The first stage operates while the clock is low and inverts and amplifies the arriving signal and charges or discharges CL1.

**Latch Timing Diagram**

Latency 32 inverter delays, Throughput = $1/(20 \times 345\text{ps}) = 0.145 \text{ GHz}$.
Latency and Throughput

Latency L is the delay between the rising edge of the clock on L0 and the data being valid internally in the last latch.

\[
L_{\text{LUMPED}} = \tau_{\text{INT}} + \tau_{\text{CPLD}} + \tau_{\text{CPLD}} + \tau_{\text{CMOS}}
\]

\[
L_{\text{PIPELINED}} = \tau_{\text{INT}} + \tau_{\text{CPLD}} + \tau_{\text{CPLD}} + \tau_{\text{CMOS}}
\]

Throughput T is the bits per second through the latches and is the maximum clock frequency.

\[
P_{\text{LUMPED}} = \frac{2}{\tau_{\text{INT}} + \tau_{\text{CPLD}} + \tau_{\text{CPLD}} + \tau_{\text{CMOS}}}
\]

\[
P_{\text{PIPELINED}} = \frac{2}{\tau_{\text{INT}} + \tau_{\text{CPLD}} + \tau_{\text{CPLD}} + \tau_{\text{CMOS}}}
\]

Basic Effective Model for a Single Rectifier

A simple effective model for a single rectifier is the "rectifier" – that is, a device that permits current to pass in only one direction. The hydraulic analog is a 'check value'. Hence the symbol:

![Diagram of a rectifier model](https://example.com/rectifier_diagram.png)

The characteristic is described as a 'rectifier' – that is, a device that permits current to pass in only one direction. (The hydraulic analog is a 'check valve'.) Hence the symbol:

![Rectifier symbol](https://example.com/rectifier_symbol.png)

Limitations of Power Consumption

- The resistive load of NMOS results in D.C. current and hence static power consumption given by the product of current times voltage.
- CMOS avoids this static loss as the pull-up device shuts off the current completely.
- CMOS still suffers a.c. power consumption that is proportional to the switching frequency.
- The energy expended per cycle of charging and discharging can never be less than \( CV^2 \)

Relation of Current to Physical Parameters

\[
I_D = \mu_N C_{\text{ox}} \left( \frac{W}{L} \right) (V_{GS} - V_T) - V_{OUT,SAT} = 0
\]

Mobility of carriers

\[
\mu_n = \frac{500 \text{cm}^2 / \text{Vs}}{\mu_p = 150 \text{cm}^2 / \text{Vs}}
\]

Oxide thickness

\[
C_{\text{ox}} = \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}}
\]

Geometrical Layout

\[
V_{OUT,SAT} = E_{\text{sat}} - L = 10^3 \left( \text{V/cm} \right) \times 0.25 \text{cm}^2 = 0.25 \text{V}
\]

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