10/29/03

EE 42 – Introduction to Electronics for Computer Science

Fall 2003, Prof. A. R. Neureuther
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UC Berkeley Office Hours M1, Tu, Tu 10:30-11:30, F 1
Course Web Site http://www-inst.eecs.berkeley.edu/~ee42/

Problem Set # 9

Due:1 PM Nov 5th, 2003 in box in 240 Cory

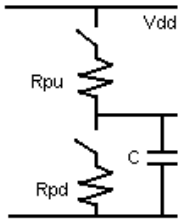
Midterm Thursday November 6th

In class, Closed Book, Closed Notes, Device Equations Provided

Review Session #1: 5 PM Tuesday Nov 4th, meet at 241 Cory

Review Session #2: 6 PM Wednesday Nov 5th, meet at 241 Cory

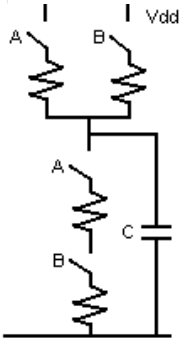
9.1 Delay in Transistor Circuits



Use the logic circuit to the right with R_{PU} = 20kΩ, R_{PD} = 10kΩ, and C = 20fF.

a) For a transition from high voltage to low voltage, where V_{DD} = 5V, determine the delay in the system.
b) For a transition from low to high voltage, determine the delay in the system.
c) What could you do to improve worst case delay by a factor of 2?

9.2 More Delay, and Delay Compensation

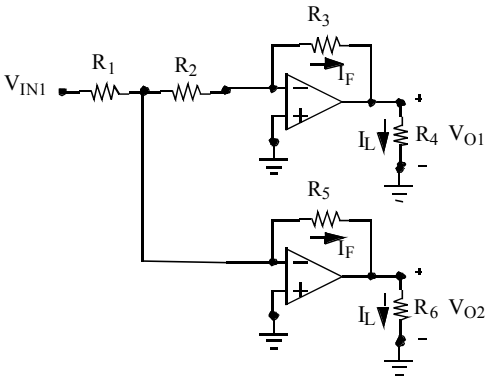


Take the following model of a logic circuit. C = 20fF.

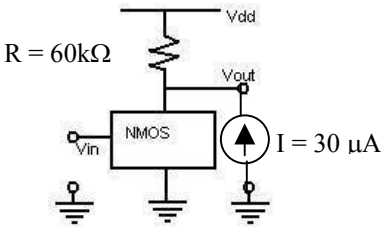
a) Determine the truth table for this circuit. What kind of logic gate is this? (Suppose A & B are input voltages controlling the switches. On pull-up, if control is low, you close the switch. On pull-down, if control is high, you close the switch. Otherwise, the switch is open)
b) Given that all resistors are 10kΩ, determine worst case delay from low to high voltage. Assume the pull-up and pull-down networks never "pull" at the same time.
c) Determine the worst case delay from high to low voltage.
d) What could you do to equalize the worst case delays? (Hint adjust the W/L to adjust the resistance.)

9.3 Review on Op-Amps

For the Op-Amp circuit to the right find V_{OUT1} and V_{OUT2} as a function of V_{IN1}. Be sure to show your fundamental assumptions. (Watch out this circuit may not be very useful.)



9.4 Review on Three Terminal Devices



Use the EE42 Device Equations. V_{DD} = 3 V and R = 60kΩ.

a) Plot the I_{OUT} vs. V_{OUT} graph for the circuit external to the NMOS.
b) Determine the NMOS current and voltage when V_{IN} = 0, 1,2, and 3V.
c) Sketch a rough plot of V_{OUT} vs. V_{IN} from your data in b).

$$I_{OUT-SAT-n} = k_n'\left(\frac{W}{L}\right)_n (V_{IN} - V_{Tn})V_{OUT-SAT-n}$$

$$I_{OUT-SAT-p} = k_p'\left(\frac{W}{L}\right)_p (V_{DD} - V_{IN} - |V_{Tp}|)V_{OUT-SAT-p}$$

	V_T(V)	$V_{OUT-SAT}$ (V)	k' (μA/V²)
NMOS	0.43	0.63	100
PMOS	0.4	1	25

For a minimum sized device W/L =2