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EECS 42
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Homework 6 Solutions

Problem 6.1. Logic and Truth Table from Circuit Symbols

a) Write algebraic expressions for the logic functions X and Y.

$$X = A + \overline{B}$$
$$Y = \overline{BC}$$

b) Combine these logic functions to find F.

$$F = \overline{XY}$$
$$F = \overline{(A + \overline{B}) \bullet (\overline{BC})}$$

c) Truth Table

A	B	C	X	Y	F
0	0	0	1	1	0
0	0	1	1	1	0
0	1	0	0	1	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	1	0
1	1	0	1	1	0
1	1	1	1	0	1

Problem 6.2. Synthesis via Sum of Products.

A	B	C	X	Y	F
0	0	0	1	1	0
0	0	1	1	1	0
0	**1**	**0**	0	1	**1**
0	**1**	**1**	0	0	**1**
1	0	0	1	1	0
1	0	1	1	1	0
1	1	0	1	1	0
1	**1**	**1**	1	0	**1**

To apply the sum of products method for the variable F, we identify rows that have 1's in the F column. We continue by creating three product terms ABC and placing a NOT over each of the variables that have a corresponding zero in the column of the variable.

$$\boxed{F = \overline{A}B\overline{C} + \overline{A}BC + ABC}$$

Note: ABC is a single product term. A NOT is placed over any of the variables that have a corresponding zero in the truth table.

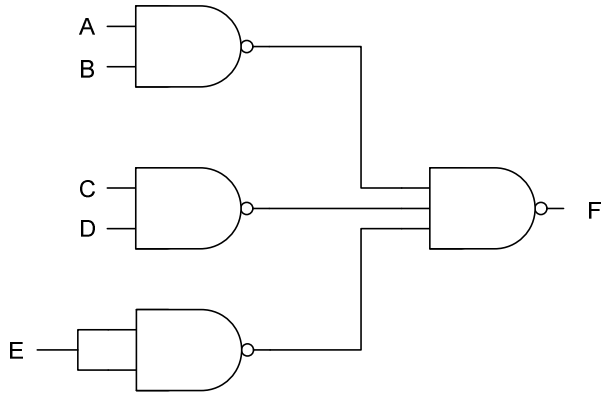
Problem 6.3. Synthesis of your own logic function.

Arbitrary logic function: $F = AB + CD + E$

a) Draw a circuit that realizes your sum of products form in NAND gates.
To generate a circuit using only NAND gates, it helps to apply DeMorgan's law to function F.

$$F = \overline{\overline{AB + CD + E}} = \overline{\overline{AB} \bullet \overline{CD} \bullet \overline{E}}$$

Note that this expression expresses all the terms using NAND functions
The gate equivalent is shown below:



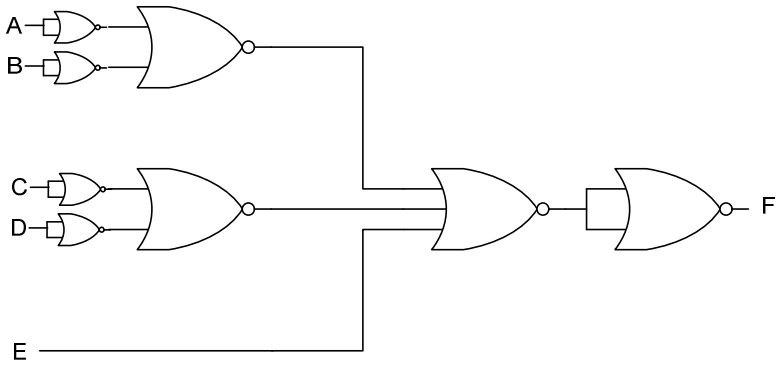
b) Apply a DeMorgan's law to convert the sum to a product

$$F = AB + CD + E = \overline{\overline{AB + CD + E}} = \overline{\overline{AB} \bullet \overline{CD} \bullet \overline{E}}$$

c) Apply the other DeMorgan's law to convert the initial products that still appear in b) to sums.

$$F = AB + CD + E = \overline{\overline{AB + CD + E}} = \overline{\overline{AB} \bullet \overline{CD} \bullet \overline{E}} = \overline{(\overline{A} + \overline{B}) \bullet (\overline{C} + \overline{D}) \bullet E}$$

d) The NOR gate representation:



Any NOR or NAND gate with a signal tied to both of its inputs will produce the inverted input signal as its output.

6.4. Timing Diagram