University of California  
Department of Electrical Engineering  
and Computer Science  

Prof. J. S. Smith  
Fall 2004  
EECS42  

Midterm  

October 18, 2004  

NAME: ___________________________  
Student ID: _________________________  

Last, First  

TA name: _________________________  

Signature: _________________________  

- CLOSED BOOK, CLOSED NOTES except one sheet, one side of notes is allowed  
- Calculators are allowed.  
- Do not un staple the exam.  
- Show all of your work and reasoning to receive full or partial credit.  
- Ask questions only if you think the problem is unclear, or there is an error in the statement of the problem.  

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1)

Consider the following circuits, and answer the questions.

![Diagram of a circuit with resistors R1=1 KΩ, R2=1 KΩ, R3=4 KΩ and a source current I=1 mA.]

**Figure 1**

1a) (5 points) In the circuit of figure 1, what is the current through R1? $I_{R1} = 1mA$

All the current from the source flows through $R_1$.

1b) (5 points) In the circuit of figure 1, what is the current through $R_2$? $I_{R2} = 0.8mA$

$I = 1mA \left( \frac{4k}{lk + 4k} \right) = 0.8mA$
1c) (5 points) In the circuit of figure 2, what is the current through the silicon diode if $V_1$ is 2 volts? 

Since the diode is non-ideal, it requires a 0.7V drop across it to turn it on.

\[ I_{\text{diode}} = \frac{2 - 0.7}{1k\Omega} = 1.3mA \]

1d) (5 points) In the circuit of figure 2, what is the current through the silicon diode if $V_1$ is 0.5 volts?

Again, the diode is non-ideal. The diode is not turned on; in fact it is reversed biased.

\[ I_{\text{diode}} = 0A \]
2) Consider the following questions, and draw an appropriate circuit in the boxes provided.

2a) (5 points) Draw a circuit which will output 2 volts when no current is drawn, and will output a current of 1mA if its outputs are shorted.

![Figure 4](image_url) Draw the circuit for question 2a here.

2b) (5 points) Using a voltage source with an output voltage of 5 volts, draw a circuit which provides an open circuit voltage of 3 volts.

![Figure 5](image_url) Draw the circuit for question 2b here.
2c) (5 points) Draw the battery charging circuit of figure 3, but add a component which will insure that the battery does NOT discharge into the voltage source if it were to fall below the battery voltage.

![Circuit Diagram](image)

Figure 6 Draw the circuit for question 2c here.

2d (5 points) Using 2 capacitors each with a capacitance of 1 microfarad, draw a circuit which will provide a total capacitance of 2 microfarads.

![Capacitor Diagram](image)

Figure 7 Draw the circuit for question 2d here.
2e) (5 points) Draw a circuit using an NPN bipolar transistor with a beta of 100, which produces a voltage gain of -10 and an input which has an equivalent resistance of 1 kohm. Ignore the voltage drop of the base-emitter diode.

![Circuit Diagram]

**Figure 8** Draw the circuit for problem 2e here

\[ R_{\text{IN}} = \frac{V_{\text{IN}}}{I_{\text{B}}} = 1k\Omega \]

\[ I_{\text{B}} = \frac{V_{\text{IN}}}{R_{\text{IN}}} = \frac{V_{\text{IN}}}{1k\Omega} \]

\[ I_{\text{C}} = \beta I_{\text{B}} = 100 I_{\text{B}} \]

\[ I_{\text{C}} = \frac{V_{\text{CC}} - V_{\text{CE}}}{R_{\text{C}}} \]

We want \( I_{\text{C}} \ll 1\text{mA} \) to reduce power requirements.

\[ \therefore \quad I_{\text{B}} = \frac{1\text{mA}}{100} = 10\mu\text{A} \]

\[ V_{\text{IN}} = I_{\text{B}} R_{\text{IN}} = (10\mu\text{A})(1k\Omega) = 0.01 \text{V} \]

\[ I_{\text{C}} = 100 I_{\text{B}} = 100(10\mu\text{A}) = 1\text{mA} \]

Choose reasonable voltage for \( V_{\text{CE}} \) start on \( V_{\text{CC}} \) which \( > 0 \) for transistor to work properly. Also let \( V_{\text{B}} = V_{\text{CE}} \) to get -10 gain.

\[ \frac{V_{\text{CC}}}{V_{\text{IN}}} = 10 \quad V_{\text{CC}} = 10V_{\text{IN}} = 100(0.01) = 0.1 \text{V} \]

\[ \text{Let} \quad V_{\text{CC}} = 5 \text{V.} \Rightarrow \quad R_{\text{C}} = \frac{V_{\text{CC}} - V_{\text{CE}}}{I_{\text{C}}} = \frac{5 - 0.1}{0.01} = 490 \text{ k\Omega} \]
3) 3a) (5 points) A PMOS transistor is used to drive an output on a logic device. When it is turned on, it has a resistance of 100 kOhm. It is used to drive a wire to other inputs, and the total capacitance of the other inputs is 10 picofarads. It is supplied from a positive rail at 3 volts. Assume that before the PMOS transistor is turned on, the capacitor is discharged (Vout=0)

![Figure 9 Circuit for problem 3](image)

Figure 9 Circuit for problem 3

![Figure 10 Equivalent circuit for problem 3 when the PMOS FET is ON.](image)

Figure 10 Equivalent circuit for problem 3 when the PMOS FET is ON.
3a) (5 points) Should the voltage at the gate of the PMOS transistor be at 3 volts or 0 volts to turn it on?

3b) (5 points) Sketch the voltage at the output as a function of time.

![Graph showing voltage over time](image)

Figure 11 Output voltage as a function of time for problem 3b

3c) (5 points) How long does the voltage take to get up to 1.5 volts?

\[ RC = 10^{-6} \]

\[ 1.5 = 3 \left(1 - e^{-\frac{t}{RC}}\right) \]

\[ 0.5 = 1 - e^{-10^6 t} \]

\[ -10^6 t = \ln 0.5 \]

\[ = -\ln 2 \]

\[ t = \ln 2 \times 10^{-6} \]

\[ = 0.69 \mu s \]
3d) (5 points) In the circuit below, the capacitor on the left is 1 picofarad, and the capacitor on the right is 10 picofarads. Just previous to t=0, the 1 picofarad capacitor is charged to 1 volt, and the 10 picofarad capacitor is discharged (no voltage across it). A switch connects them in series with a resistance of 1 kohm at time t=0. Find the voltage that the 10 picofarad capacitor will have across it after a long time. \[ V_{C2} = \frac{V_{1}}{11} \]

![Circuit Diagram](image)

**Figure 12 circuit for problem 3d and 3e**

\[ Q = 1 \text{pf} \times 1 \text{V} = 1 \text{p} (\text{C} \cdot \text{V}) \]

\[ Q = Q_1 + Q_2 = 1 \text{p} = C_1 V_1 + C_2 V_2 \]

\[ t \to \infty, \quad V_1 = V_2 \]

\[ 1 \text{p} = (C_1 + C_2) V_2 \]

3e) What is the RC time constant of the circuit from problem 3d and figure 12?

**Capacitors are in series**

\[ C_{eq} = \frac{1 \text{p} \cdot 10 \text{p}}{1 \text{p} + 10 \text{p}} = \frac{10}{11} \text{p} \]

\[ \tau = RC = 1 \text{k} \times \frac{10}{11} \text{p} = 0.91 \times 10^{-9} \text{s} \]

\[ \tau_{RC} = 0.91 \times 10^{-9} \text{s} \]
4a) (5 points) Explain what a “hole” in a P type semiconductor is.

In a p-type semiconductor, some silicon atoms are replaced with group 3 elements, with only 3 valence electrons. The “missing” electron, that is, the spot that can be filled by an electron, behaves as if it were a positively charged particle, a “hole”.

4b) (5 points) In a “depletion layer” in a semiconductor device, what is “depleted”?

At the junction between p-type and n-type semiconductors, the majority carriers from one side [ holes in the p-type and electrons in the n-type ] diffuse across the boundary and combine with the majority carriers from the other side. This gives rise to the depletion region, the zone where the majority carriers have thus been depleted.

4c) (5 points) Explain why a PN diode can conduct current in one direction, but not in the reverse direction.

A forward bias across a pn junction [ with a positive voltage applied to the p-type side ] causes the majority carriers to be pushed towards the junction, decreasing the size of the depletion layer. Above a certain potential, the carriers have enough energy to make it across the depletion layer and carry current through the device. In reverse bias, the carriers are pulled away from the junction, thus increasing the required energy to cross the depletion layer, resulting in negligible current.

4d) (5 points) Explain what “ripple” is in a power supply, and how it can be reduced.

Power supply ripple is the oscillating variation in DC output voltage of a rectifier caused by the oscillating AC input voltage. Filtering the output with a capacitor reduces the ripple in inverse proportion to its capacitance. Thus a larger capacitor results in smaller ripple.

4e) (5 points) Explain how a Bipolar transistor can use a small current to control a larger current.

A small current through the emitter-base diode of a npn transistor puts it in forward bias. Thus, electrons can flow from the emitter into the base. However, the base is lightly doped and thin. This means the electrons have a long lifetime in the base, as well as a short distance to go to enter the collector. Thus most of the electrons continue on to the collector, resulting in a much larger current from collector to emitter.