Problem Set 7
Due Wednesday, November 3, 5:00pm, box in Cory 240

Figure 1

Figure 2

Figure 3
1 Logic and Truth Table from Circuit Symbols. Consider the circuit in Fig. 1
   a) Write algebraic expressions for the logic functions X and Y.
   b) Combine these logic functions to find F.
   c) Evaluate the entries in a truth table for X, Y and Z as computed
      from A, B and C sequencing through their values.

2 Synthesis via Sum of Products. Use a sum of products form to
    synthesize the truth table you obtained in Problem 1.

3 Rise and fall times Using a resistance per gate of 10Kohms,
   and a capacitance per gate of .01 pf, and assuming a load of 4
   gates at the output, plot a the voltage vs time for a transition of
   the output from low to high, and another plot for high to low.

4 Timing Diagram. Use the circuit in Fig. 2. Note that this is not a good circuit as this circuit
   could be replaced by a single NAND gate. Assume that B = 0 and A has been zero for a long time
   and is then switched to 1 at t = 0. Draw the timing diagram for this circuit for 4 gate delays
   assuming each gate has an identical delay of 1 ns. (You should observe that this gate ‘glitches’ in
   that the output temporarily switches to an incorrect value and then returns to the correct value.
   This of course wastes energy. Glitching accounts for about 30% of the energy consumed in logic
   circuits such as cell phones, microprocessors, etc.).