Problem set 9
Due Wednesday, November 17, 5:00pm, in the box in Cory 240

1) Implement (draw) the following using CMOS transistors.
   
   a) A single stage 3-input NOR gate. Label the inputs as a, b, and c, and the output as Q.
   
   b) Another 3-input NOR gate, this time by cascading 2 2-input NOR gates.

2) Draw a circuit implementing \( Y = \overline{A(B + C)} \), using only 3 n-type and 3 p-type MOS transistors:

3) Draw a circuit implementing a 2-input NAND-gate with tri-state output. (A tri-state output floats, i.e. it neither pulls the output up or down, when not enabled) Inputs a, and b are the normal NAND inputs; en (enable) controls the “state” of the output as in a tri-state buffer (these are the only signals available – if you need more then add circuitry to generate them). Use as few transistors as necessary. Label all inputs and outputs as with the symbols given.
4) Name the function performed by the following circuits. Draw its common symbol or state the equivalent Boolean expression.
5) Consider the D-type edge-triggered flip-flop shown.
   a) Assuming zero setup and clock-to-Q delay, draw the waveform
      for the signal at node Q.

   b) What is the function of the X signal?