a) Gate 1: \( V_{out-1} = A_1B_1 + A_2E_2D_2 + C_1D_1 + E_1E_2 \)

Gate 2: \( V_{out-2} = A_2B_2 + A_2C_2D_2 \)

b) 1. Pull-up & pull-down networks are duals of each other
2. Nmos turned on by "1", Pmos turned on by "0"
3. 

c) Gate 1:

\[ A_1, E_1, B_1 = 1; \text{others} = 0 \]

\[ \text{Max: } A_2, C_2, D_2 = 1; B_2 = 0 \]

\( C \rightarrow \text{50} \mu F \)

\( \text{Delay} = 0.69T = 0.69 \times 30 \times 5000 = 104.25 \mu s \)

\( \text{Min: } A_1, B_1, C_1, D_1 = 1; E_1 = 0 \)

\( C \rightarrow \text{50} \mu F \)

\( \text{Delay} = 0.69 \times 10 \times 5000 = 345 \mu s \)

Compared to simple inverter delay, \( D_{inv} = 345 \mu s \)

Gate 1: \( 1x - 3x \)

Gate 2: \( 1.6x - 3x \)
10.1

\( d \) Gate 1:

Max: \( A, E, D = 0 \); other inputs = 1

\[ \text{Delay} = 1.04 \text{nS} \]

Min: \( A, C, B, E = 0 \); \( E = 1 \)

\[ \text{Delay} = 3 \text{ps} \]

Compared to inverter delay: \( D_{\text{inv}} = 3 \times 5 \text{ps} \)

\[ \text{Gate 1: } 1 \times -2 \times \]

\[ \text{Gate 2: } 0.6 \times -2 \times \]

\( \text{Maximum} = 3 \times \)

10.2

(assuming load is always \( 50 \text{\Omega} \), regardless of which other transistors it is connected to)

\( a \) Assume prop. delay includes delay through gate 1: Assign primary inputs

\[ t = 552 \text{ps} \]

\[ \text{Gate 1: } A, C, E, D : 0 \rightarrow 1 \ @ t = 0 \]

\[ E : 0 \rightarrow 0 \]

\[ \text{Gate 2: } B, C, E, D : 1 \rightarrow 0 \ @ t = 345 \text{ps} \]

Want min prop delay of 345 ps (from 10.1) \( \frac{1}{2} \)

Total delay = 345 + 207 = 552 ps
10.7

b) 

> want pop delay to be max of 1.04us 
> also want max delay of 1.04us 

\[ t = 2.08 \text{us} \]

\[ \text{Total delay} = 2.08 \text{us} \]

10.8

a) Propagation delay: \( \text{CLK} \rightarrow Q \) delay:

\[ \text{Delay} = 690 \text{ps} \]

This is actually a positive edge triggered flip flop. The \( \text{CLK} \rightarrow Q \) delay is the time for the second latch to transmit its value to \( Q \), after \( \text{CLK} \) transitions from 0 to 1.

*Same value for both high to low and low to high*
b) \[ t=0 \]

- \[ \text{Releases } B_1 \]
- \[ \text{All other inputs } \]
- \[ \text{are stable; worst case path in FV} \]
- \[ \text{by all inputs are } 1. \]
- \[ \text{Get decay value from } 10.1 \]
- \[ \text{Decay value from 10.1} \]

Timing Diagram:

- \[ 1.0 \mu s \]
- \[ 0.1 \mu s \]
- \[ 3.45 \mu s \]
- \[ 6.9 \mu s \]

\[ V_{ct} \]
\[ V_{ut1} \]
\[ V_{ut2} \]
\[ V_{ct} \]

Assume \( V_{ut} = 0 \) at \( t=0 \)

Could also be \( k = 1 \)
c) \( T = 6.9\,\text{ms} \)

Timing Diagram:

- **Cke**
- **Vin**
- **Vout1**
- **Vout2**

- **Vout1** changes at 1.045\( T \)
- **Vout2** changes at 6.999\( T \)
- **Vout2** changes at 5.75\( T \)

**Note:** The timing diagram includes several events labeled with specific time points relative to the period \( T \).
10.4

a) This is from \( \text{V}_{IN\text{P}} \) to \( \text{V}_{OUT\text{P}} \). Setup time

\[
T_{\text{setup}} = t_{\text{CEO}} + t_{\text{MAXq1}} + t_{\text{MAXq2}} + t_{\text{SU}}
\]

\[
> 690ps + 1.04ns + 1.04ns + 690ps = 3.46\text{ns}
\]

from 10.1 and 10.3a just the delay through \( \frac{1}{2} \) of the flip-flop.

b) Max delays of both subsection are the same

\[
= t_{\text{CEO}} + t_{\text{MAXq}} + t_{\text{SU}} = 2.42\text{ns}
\]

c) Lumped: Latency = CLK period = 6.96\text{ns} or 20x

\[
\text{Pipelined: } \frac{1}{8.17\text{ns}} \quad \text{or} \quad \frac{1}{23.78}\text{ns}
\]

\[
\text{Lumped: } \frac{1}{3.35\text{ns}} \quad \text{\Rightarrow 289 MHz}
\]

\[
\text{Pipelined: } \frac{1}{2.42} \quad \text{\Rightarrow 413 MHz}
\]

\[
\text{Pipelined is } \frac{413}{289} \text{ "faster"}
\]

\[
\text{Duty cycle doesn't matter if } \frac{1}{F_{\text{in}}}
\]