UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
and Computer Sciences

Professor Oldham

Fall 2002

EECS 42 — Final Exam

SOLUTIONS

Friday, 13 December 2002, 12:30-3:30 p.m.

Name: _____ **Student ID:** _____

Last, First

Signature: _____

Guidelines:

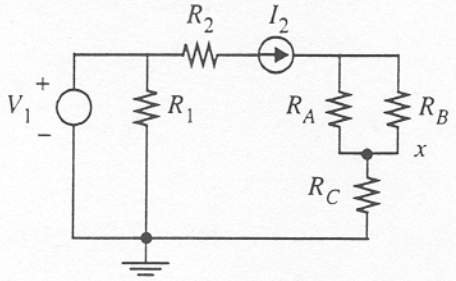
1. Closed book. A summary with formulas is provided at the end of the exam.
2. Show ***all your work and reasoning on the exam*** in order to receive credit.
3. **Warning**: Some problems will be graded with no partial credit, so check your answers and be sure to put answers in boxes provided.
4. You may use a calculator.
5. Do not unstaple the exam. There are 2 blank pages at the end if you need more workspace.
6. This exam contains 8 problems and corresponding worksheets plus the cover page and the 4-page summary with formulas.
7. **Please do not ask questions** except to point out possible errors or typographical mistakes.

Problem	Points Possible	Your Score	Problem	Points Possible	Your Score
1	25		5	25	
2	30		6	20	
3	25		7	25	
4	25		8	25	
			Grand Total	**200**	

f	10^{-15}
p	10^{-12}
n	10^{-9}
μ	10^{-6}
m	10^{-3}
K	10^{3}
M	10^{6}

Problem 1 (25 points)

(a)

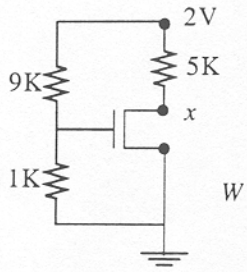


$V_x = I_2 R_C$

Check "Yes" or "No" for each item in the following table:

		Yes	No
V_x depends on	V_1 ?		✓
"	R_1 ?		✓
"	R_2 ?		✓
"	R_A ?		✓
"	R_B ?		✓
"	R_C ?	✓	

(b)



$V_T = 1\text{V}$

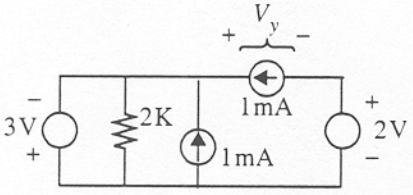
$W \cdot I_{DS}' = 0.1\text{mA/V}$

$\lambda = 0.1\text{V}^{-1}$

Find V_x.

$V_x =$ 2 (V)

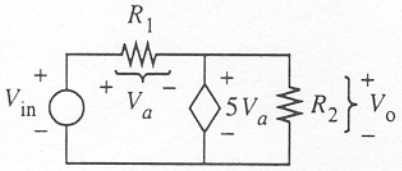
(c)



Find V_y.

$V_y =$ −5 (V)

(d)



Find V_o in terms of V_{in}, R_1, R_2.

$V_o = \frac{5}{6} V_{in}$

$V_o = 5V_a \qquad V_a = V_{in} - V_o$

$= \frac{1}{6} V_{in}$

$V_o = 5(V_{in} - V_o)$

$= \frac{5}{6} V_{in}$

Problem 2 (30 points)

We are going to analyze the circuit of Figure 2. The op-amp model, valid in the linear region, is given in Figure 1. The linear region is bounded by the rails at 0V, 9V.

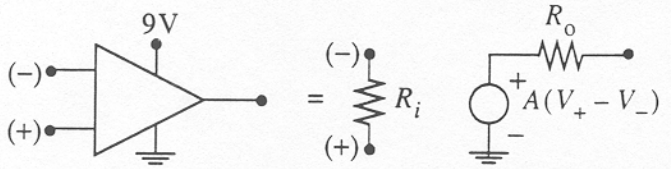


Figure 1

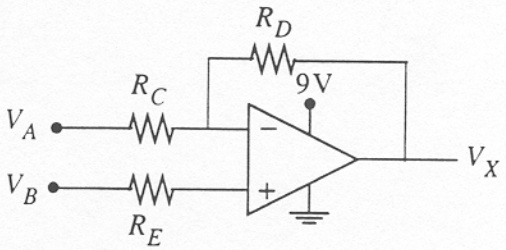


Figure 2

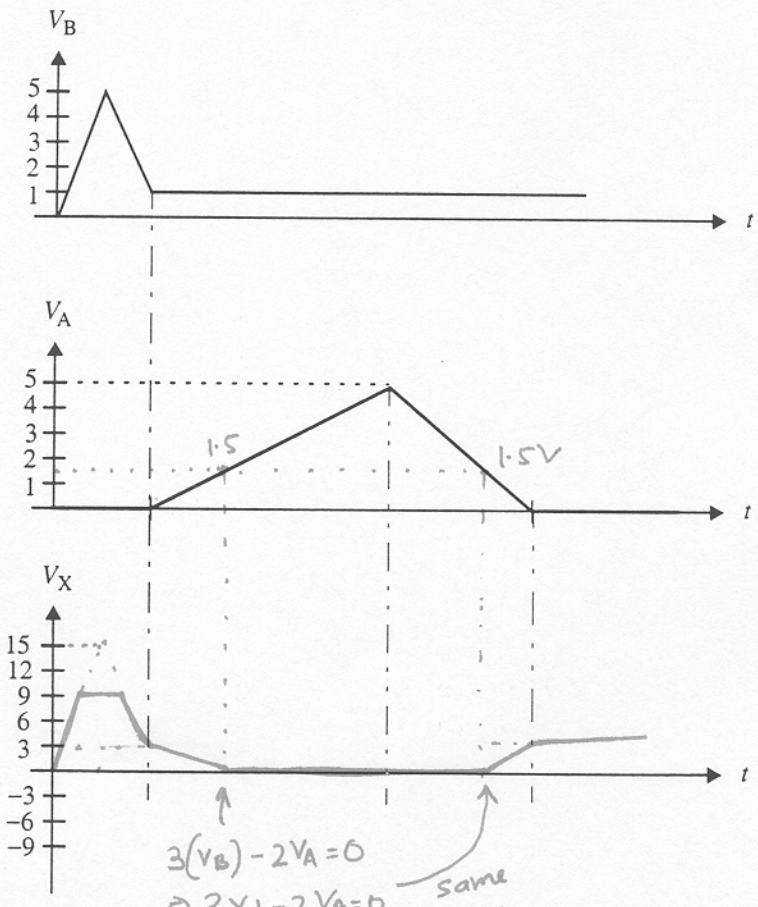
(a) For the op-amp circuit of Figure 2, derive the equation relating V_X to V_A and V_B in the linear region. Assume $R_o = 0, R_i = \infty$. You must show your work (use page 4).

$V_X =$ $\dfrac{A.\left(V_B(R_C+R_D) - V_A R_D\right)}{R_C + R_D + A R_C}$

(b) What does this become in the limit $A \to \infty$?

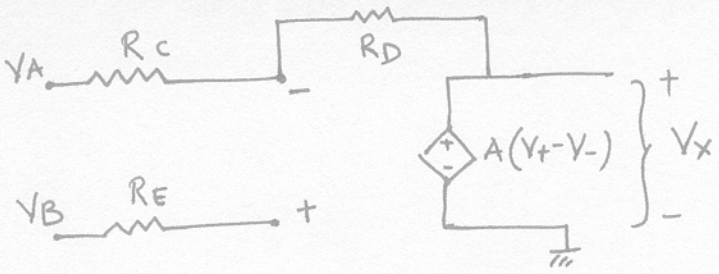
$V_X =$ $V_B + \dfrac{R_D}{R_C}(V_B - V_A)$

(c) Assume that for some values of R_C, R_D and R_E, the equation for V_X is $V_X = 3V_B - 2V_A$ (which need not be correct for the circuit given). Given V_A and V_B waveforms below, show the waveform for V_X.



Rails at 9V & 0V respectively

Problem 2 Worksheet



part (a)

$$V_x = A(V_+ - V_-) \quad \ldots\ldots (i)$$

$$V_+ = V_B \quad \ldots\ldots (ii)$$

$$V_- = V_A + \frac{(V_x - V_A) R_C}{R_C + R_D} \quad \ldots\ldots (iii)$$

from (i), (ii) & (iii), we get -

$$V_x = A\left(V_B - \left(V_A + \frac{(V_x - V_A) R_C}{R_C + R_D}\right)\right)$$

$$\Rightarrow V_x\left(\frac{1}{A} + \frac{R_C}{R_C + R_D}\right) = V_B - V_A + \frac{V_A R_C}{R_C + R_D}$$

$$\Rightarrow V_x\left(\frac{R_C + R_D + A R_C}{A(R_C + R_D)}\right) = \frac{V_B(R_C + R_D) - V_A R_D}{(R_C + R_D)}$$

$$\Rightarrow \boxed{V_x = A.\left[\frac{V_B(R_C + R_D) - V_A R_D}{R_C + R_D + A R_C}\right]} \quad \text{Ans.}$$

part (b)

$$\lim_{A \to \infty} V_x = \lim_{A \to \infty} \frac{A\left(V_B(R_C + R_D) - V_A R_D\right)}{R_C + R_D + A R_C}$$

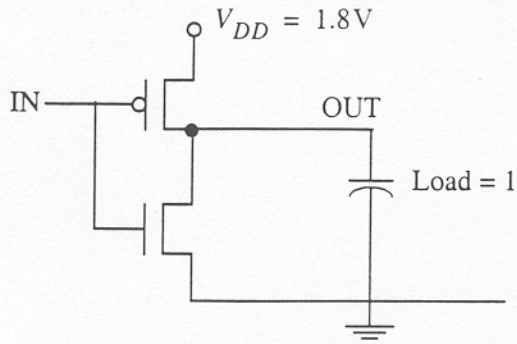
$$= \lim_{A \to \infty} \frac{V_B(R_C + R_D) - V_A R_D}{\frac{(R_C + R_D)}{A} + R_C}$$

$$\Rightarrow V_x = \frac{V_B(R_C + R_D) - V_A R_D}{R_C}$$

$$\Rightarrow \boxed{V_x = V_B + \frac{R_D}{R_C}(V_B - V_A)} \quad \text{Ans.}$$

Problem 3 (25 points)

The CMOS inverter shown must drive a load (which is a very long line on the chip) with a capacitance of 10 pF. We require that both the rising and falling stage delays be 0.5 nsec.



Standard 0.18µm CMOS Inverter

The device properties are given in Lecture 22 summary at the end of the exam. But for this problem use $\lambda = 0$.

(a) What value of R_P and R_N are required to achieve the 0.5nsec stage delay?

$R_P = R_N = R$

$0.69\,RC = 0.5\times10^{-9}$ sec

$C = 10\times10^{-12}$ F

$\Rightarrow R = 72.5\,\Omega$

R_P =	72.5 Ω
R_N =	72.5 Ω

(b) Suppose the answer to part A were $R_P = 100\Omega$, $R_N = 100\Omega$ (not the right answers!). What NMOS and PMOS device widths would be required? (Standard 0.18µm device properties, but with $\lambda = 0$.)

$R_P = R_N = \dfrac{0.75\,Vdd}{I_{AVE} = I_{DS_{\lambda=0}}} = \dfrac{0.75\times1.8}{W\cdot I_{DS}'\cdot|V_{GS}-V_T|}$ $V_{GS}=1.8$, $V_T=0.4$

$R_N = 100$, $W_N = 19.3\,\mu m$

$R_P = 100$, $W_P = 38.6\,\mu m$

$\Leftarrow$ $\rightarrow 500\times10^{-6}$ (NMOS), 250×10^{-6} (PMOS)

W_P =	38.6 µm
W_N =	19.3 µm

(c) At what input voltage does the maximum current flow from V_{DD} to ground?

At $V_{in} > \frac{1}{2}Vdd$, both transistors are on "half-way" and current flows through $V_{DD} \rightarrow$ Ground (cap. is irrelevant)

V_{IN} =	0.9V

(d) What is the value of the current?

$\lambda=0$, $I_D = I_{DS} = W\times I_{DS}'\times|V_{GS}-V_T|$

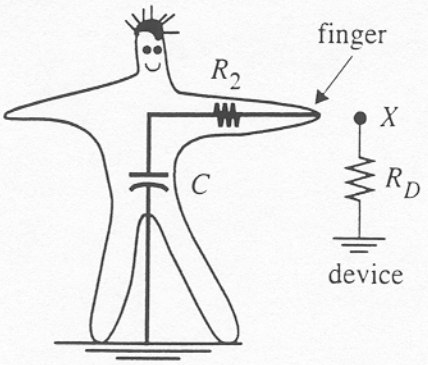
$= 19.29\times500E^{-6}\times(0.9-0.4)$

$= 4.82$ mA

I =	4.82	mA

Problem 4 (25 points) – Please give answers on page opposite

As you may know, electrostatic discharge can destroy CMOS circuits by "zapping" the gate insulators. The equivalent circuit of a Berkeley undergraduate on a nylon carpet is given below:



$R_2 = 100\text{K}\Omega$

$C = 20\text{pF}$

Undergrad Circuit Model

Suppose C is initially charged to 25KV by a short walk on the carpet.

(a) What is the energy stored in the capacitor?

(b) Let R_D represent a device you touch at $t = 0$ (finger touchs X, connecting R_2 to R_D). $R_D = 25\text{K}\Omega$. Sketch the voltage on node X versus time.

(c) Write an equation for the voltage $V_X(t)$.

(d) Your strategy to protect the device is to put a series resistance R_S on your finger so big that V_X never rises above 10 V. (That is, R_S is in series with R_2.)

How big must R_S be?

Problem 4 Answer Sheet

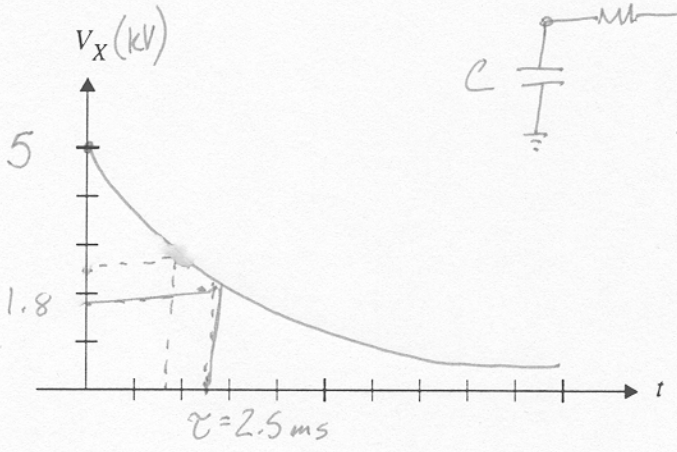
(a)

$$E = \frac{1}{2}CV^2 = \frac{1}{2}(20\times10^{-12}\,F)(25\times10^{3}\,V)^2$$

$$= 6.25\,mJ$$

E = 6.25 mJ

(b)



from Voltage divider formula,

$$V_X = V_C \frac{R_D}{R_2+R_D}$$

$$V_X(0) = V_C(0)\frac{R_D}{R_2+R_D}$$

$$= (25\,kV)\frac{25k}{100k+25k}$$

$$= 5\,kV$$

(c)

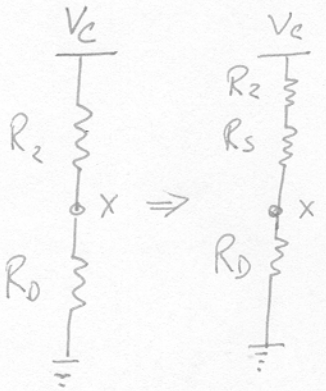
Capacitor is discharging

$$V_X(t) = \frac{R_D}{R_2+R_D}V_C(t) = \frac{R_D}{R_2+R_D}(25kV)e^{-t/2.5ms}$$

$$= (5kV)e^{-t/2.5ms}$$

$V_X(t)$ = $(5kV)e^{-t/2.5\,ms}$

(d)



$$V_x = 25kV\frac{R_D}{R_2+R_D+R_S}$$

$$10V = (25kV)\frac{25k}{25k+100k+R_S}$$

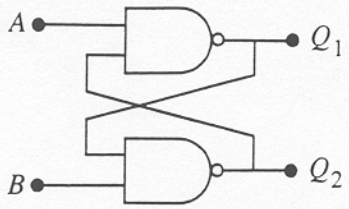
$$25k+100k+R_S = (25k)\frac{25kV}{10V}$$

$$R_S = 62500k - 125k = 62{,}375k$$

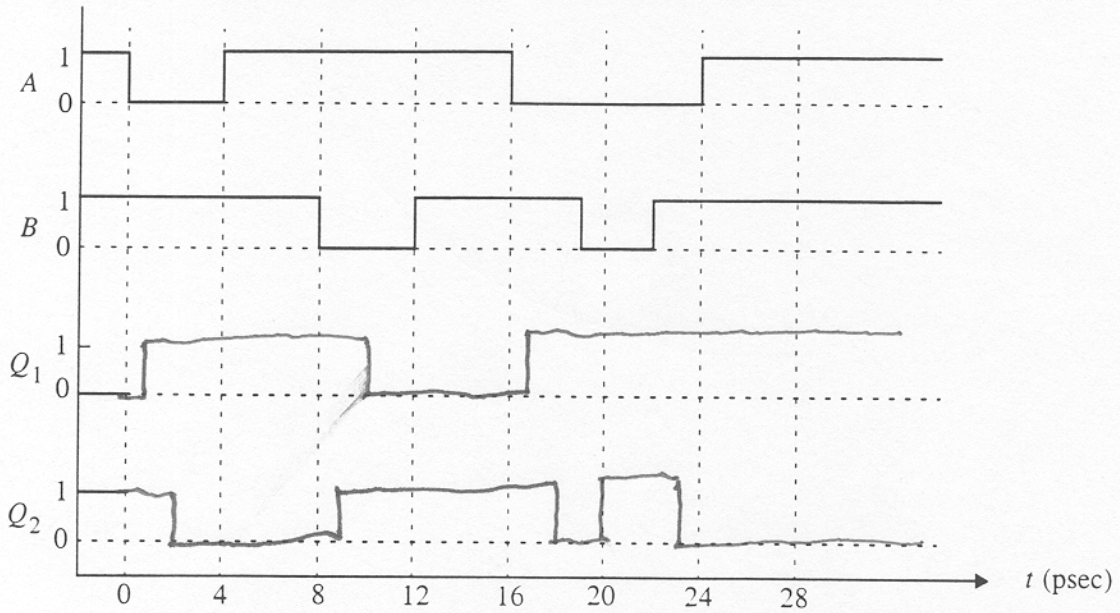
R_S = 62.375 MΩ

Problem 5 (25 points)

A non-standard flip-flop circuit is given below:



(a) A possible set of input waveforms is given below. Show the behavior of Q_1 and Q_2 assuming the unit gate delay is 1 psec. (Do **NOT** ignore gate delay in your diagram.)



(b) Under what input conditions is $Q_2 \neq \overline{Q}_1$?

A =	0
B =	0

(c) Under what input conditions is $Q_2 = \overline{Q}_1$ and Q_1 is free to be either 0 or 1 (depending on previous history)?

A =	1
B =	1

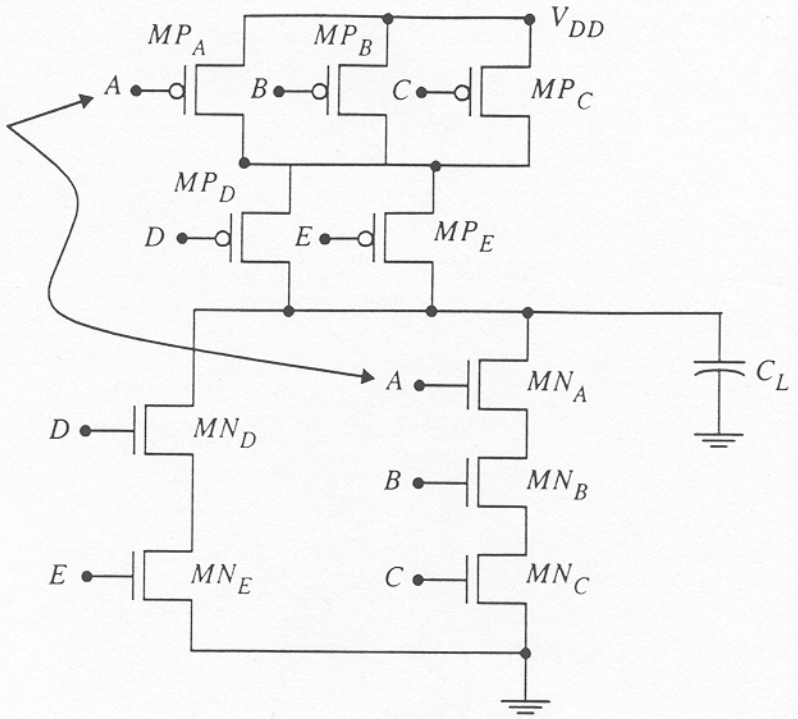
(d) How many PMOS and NMOS devices would it take to construct this circuit?

NMOS	4
PMOS	4

Problem 6 (20 points)

The following special CMOS logic circuit is constructed in our standard 0.25μm CMOS.

Note: A is actually connected to A, etc., but these wires are omitted for simplicity.



(a) Write the expression for the logic function $\bar{F}$ in terms of A, B, C, D, E.

$\bar{F} =$ ABC + DE

(b) Assume devices MN_D and MN_E are 2μm wide, size all the remaining devices so that they are as small as possible, but the worst case fall time equals the worst case rise time, i.e., find all device widths.

$W_{MP_A} =$ 4um $\quad W_{MN_A} =$ 3um

$W_{MP_B} =$ 4um $\quad W_{MN_B} =$ 3um

$W_{MP_C} =$ 4um $\quad W_{MN_C} =$ 3um

$W_{MP_D} =$ 4um

$W_{MP_E} =$ 4um

Problem 7 (25 points)

The I-V graph of a super high performance experimental NMOS device is given in Figure 1. The device Width is $W = 1\mu m$.

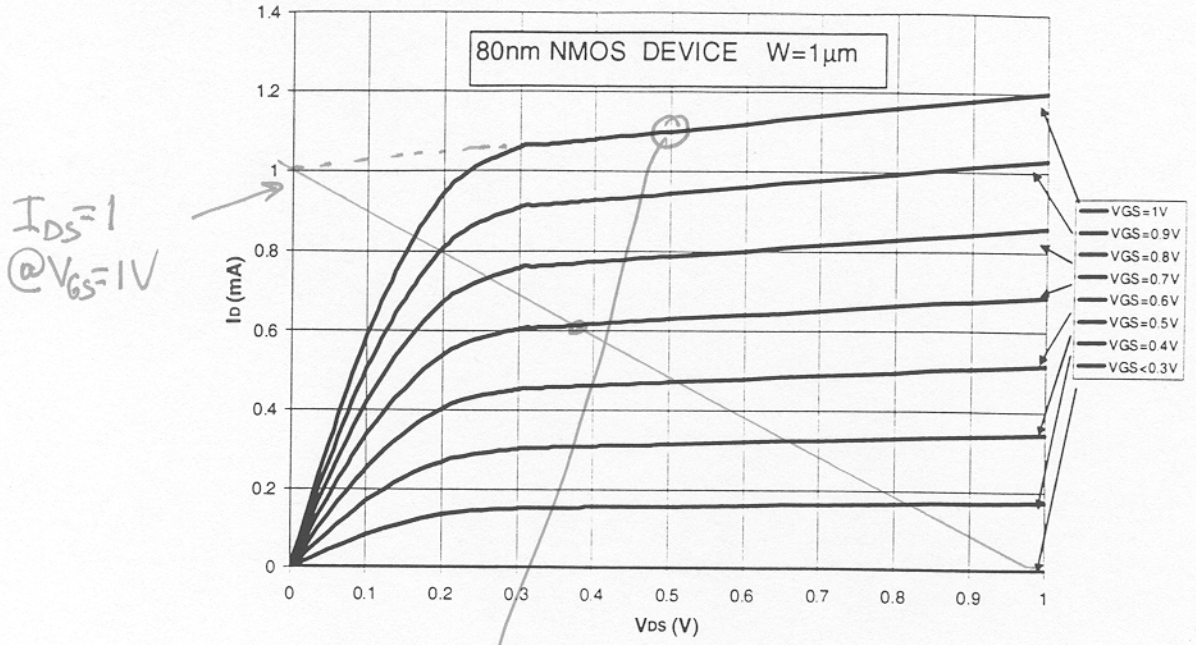


Figure 1

(a) What is I_D if $V_{GS} = 1V$, $V_{DS} = 0.5V$ (±10%)? → 1.1 mA

$I_D =$ 1100 µA

(b) Can you estimate values for V_T? $I \to 0$ at $V_{GS} \to V_T$ ≈ 0.3 V

$V_T =$ 0.3 V

(c) What is the value of the parameter I_{DS}' for this device (±10%)?

$I_{DS} = W I_{DS}' (V_{GS} - V_T) \Longrightarrow$ (I_{DS} = 1 mA, $V_{GS} - V_T$ = 0.7)

$I_{DS}' =$ 1400 µA/V·µm

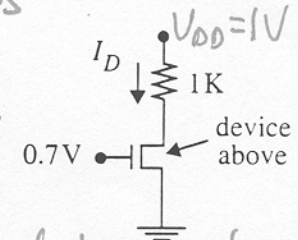
(d) What is the value of the parameter λ for this device (±20%)?

$-\lambda = 1/$ INTERCEPT OF STRAIGHT LINE

$I_D = 1 + 0.2\,mA/V \cdot V_{DS} \to$ INTERCEPT = −5V

$\lambda =$ 1/5 = 0.2 V^{-1}

(e) What is I_D in this circuit?



See load line above

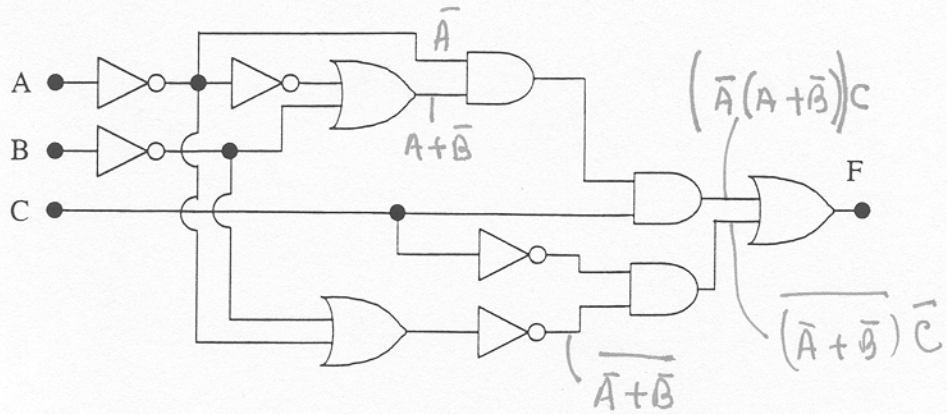
$V_{DS} = .35V$

$I_D = .61\,mA$

$I_D =$ 0.61 mA

Problem 8 (25 points)

A recent Stanford graduate performed a logic design and proudly came up with the following logic circuit:



(a) Write the logic function directly from the circuit without simplification (please, without simplification). There is only one correct answer for this part, even though you may greatly simplify the expression with little effort.

(b) Simplify the expression for F.

(c) The answer to part (c) is not $A\bar{B}+\bar{A}BC$, but for this part of the problem we will assume that the answer to part (c) is $F = A\bar{B}+\bar{A}BC$. Design a logic circuit for this function using only NAND gates, with inputs A, B, C and output F.

Problem 8 Answer Sheet

(a)

$$F = (\bar{\bar{A}} + \bar{B})\bar{A}C + \overline{(\bar{A} + \bar{B})}\,\bar{C}$$

(b)

$$F = (\bar{\bar{A}} + \bar{B})\bar{A}C + \overline{(\bar{A} + \bar{B})}\,\bar{C}$$
$$= (A + \bar{B})\bar{A}C + \overline{(\bar{\bar{A}} \cdot \bar{\bar{B}})}\,\bar{C}$$
$$= A\bar{A}C + \bar{B}\bar{A}C + AB\bar{C}$$
$$= \bar{B}\bar{A}C + AB\bar{C}$$

$$F = \bar{B}\bar{A}C + AB\bar{C}$$

(c) Draw circuit here: