

Introduction to Digital Systems

Today: (12)

- Bits and bytes
- Small digital systems
- Digital signal processing

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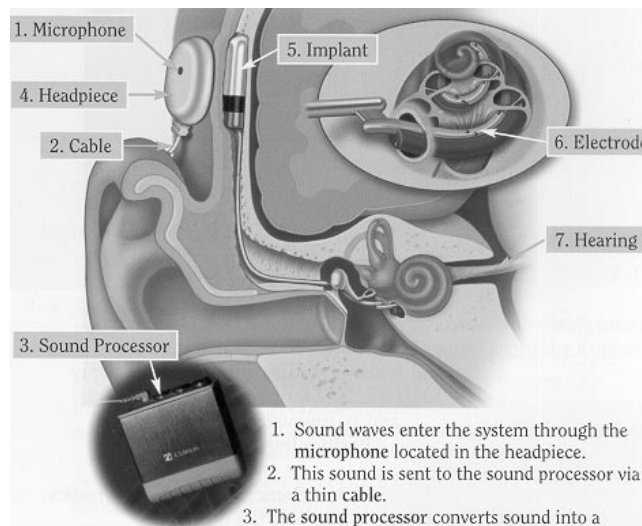
So Why Digital?

(For example, why CDROM audio vs vinyl recordings?)

- Digital signals can be transmitted, received, amplified, and re-transmitted with no degradation.
- Binary numbers are a natural method of expressing logical variables.
- Complex logical functions are easily expressed as binary functions (e.g., in control applications ... see next page).
- Digital signals are easy to manipulate (as we shall see).
- With digital representation, we can achieve arbitrary levels of “dynamic range,” that is, the ratio of the largest possible signal to the smallest than can be distinguished above the background noise
- Digital information is easily and inexpensively stored (in RAM, ROM, EPROM, etc.), again with arbitrary accuracy.

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Cochlear Implant

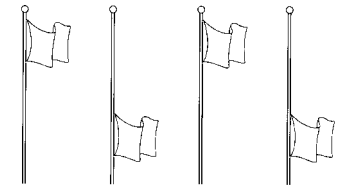


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How do you represent number digitally?

10V in decimal becomes:

- “13” in base 7
- “14” in base 6
- “22” in base 4
- “1010” in Binary (base 2)

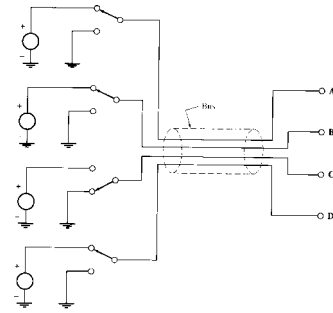
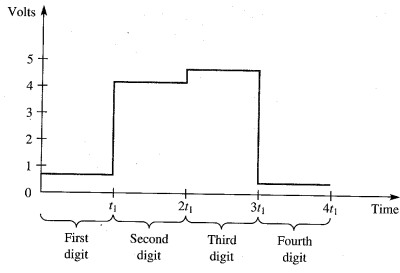


- A binary digit (bit) can store 0 or 1 and can be stored in a flip flop
- 4-bit can store number between 0000 to 1111 (16 different numbers)
- N-bit can store 2^N different numbers. (8 bit can store 256, 10 bit → 1024, 15 bit → 32768 ($2^5 \times 1024$)...)

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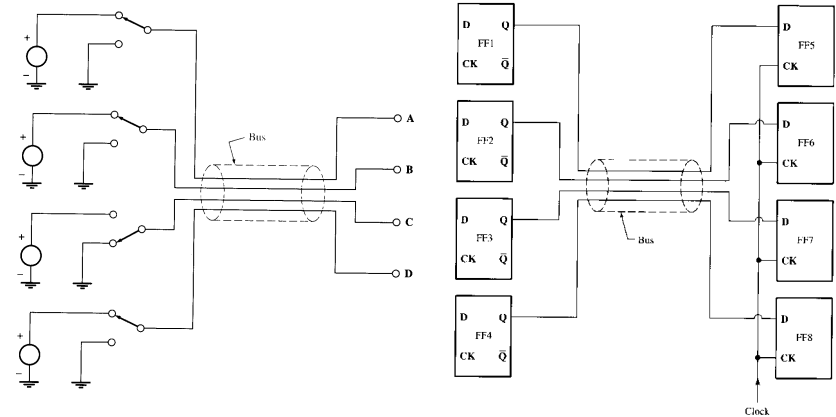
Binary transmission

- Suppose we need to transmit 4 bit in binary.
- We can transmit 4 bit **serially** (one bit at a time) or **simultaneously** (four bit together)



4-bit flip flops or registers

- 4 bits are transmitted simultaneously, but 4-bit byte is transmitted serially.
- FF5-FF8 are called the storage register or data latch.



Decimal, binary, and hexadecimal number

- Convert from decimal to binary
- $245_{10} = 11110101_2$

Decimal number to be converted	Quotient	Remainder
$245 \div 2$	122	1
$122 \div 2$	61	0
$61 \div 2$	30	1
$30 \div 2$	15	0
$15 \div 2$	7	1
$7 \div 2$	3	1
$3 \div 2$	1	1
$1 \div 2$	0	1

Binary result
 $245_{10} = 11110101_2$

- Convert from binary to decimal

$$\begin{aligned}
 11110101_2 &= 1 \times 2^7 + 1 \times 2^6 + 1 \times 2^5 + 1 \times 2^4 \\
 &\quad + 0 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 \\
 &= 128 + 64 + 32 + 16 + 0 + 4 \\
 &\quad + 0 + 1
 \end{aligned}$$

Decimal, binary, and hexadecimal number

- It is clumsy to write 11110101_2
- Can change it into hexadecimal (base 16)
- $11110101_2 = ?$ 16
- Convert from hexadecimal to binary?
- Convert from hexadecimal to decimal?
 - $AEC_{16} = ?$ 10
 - $AEC_{16} = ?$ 2
- Convert from decimal to hexadecimal?
 - $245_{10} = ?$ 16

Decimal	Binary	Hexadecimal
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F
16	10000	10
17	10001	11
18	10010	12
19	10011	13
⋮	⋮	⋮

Decimal, binary, and hexadecimal number

- Multiplication ?

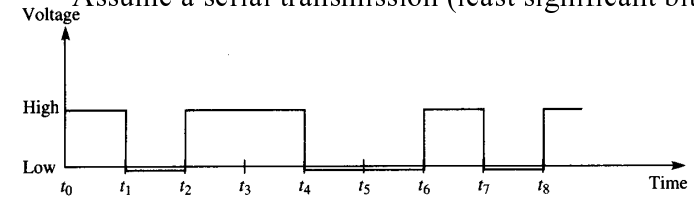
$9C_{16} \times A3_{16} = ?$

$$\begin{array}{r}
 9C_{16} = \quad 1001\ 1100 \\
 A3_{16} = \quad 1010\ 0011 \\
 \hline
 \quad 1001\ 1100 \\
 \quad 1\ 0011\ 100 \\
 \quad 1\ 0011\ 100 \\
 \hline
 100\ 1110\ 0 \\
 \hline
 110\ 0011\ 0101\ 0100 \\
 \hline
 6\ 3\ 5\ 4 = 6354_{16}
 \end{array}$$

Small digital systems

- Shift registers

– Assume a serial transmission (least significant bit first)

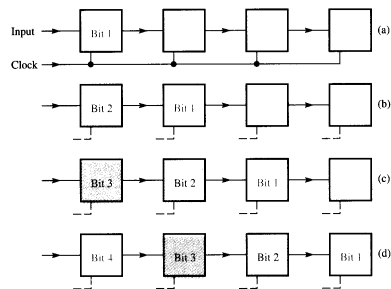


Represents 01001101 or $4D_{16}$

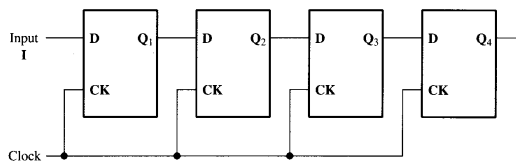
We need to look at the 8 bit in order to something about it. What we need is shift registers.

Small digital systems (shift registers)

- Bit is shift to the right 1 clock cycle at a time

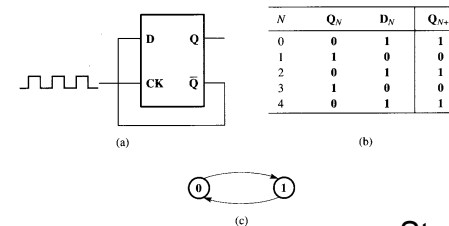


- A 4-bit shift register can be implemented by 4 D flaps flops connected serially -- output Q1 of the 1st FF is connected to the input D2 of the 2nd FF.

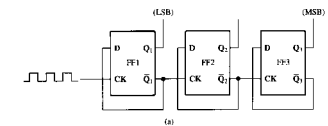


Counter

1-bit counter



N	Q _N	D _N	Q _{N+1}
0	0	1	1
1	1	0	0
2	0	1	1
3	1	0	0
4	0	1	1

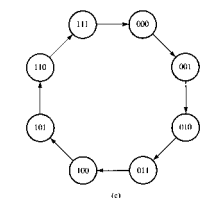


State table

N	Q _{2v}	Q _{1v}	Q _{0v}	(Q ₂ Q ₁ Q ₀) _v
0	0	0	0	000
1	1	0	0	001
2	0	1	0	010
3	1	1	0	011
4	0	0	1	100
5	1	0	1	101
6	0	1	1	110
7	1	1	1	111
8	0	0	0	000

- 3-bit ripple counter

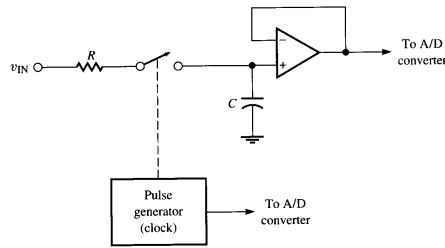
State diagram



Digital Signal Processing

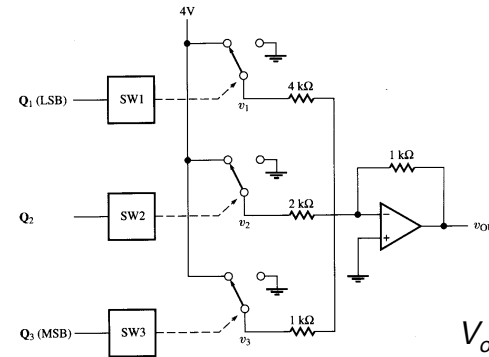
- Analog signal → digital signal
(need Analog to Digital converter or A/D converter)
- Sampling
- Nyquist sampling theorem

$$T_s < 1/(2f_{max})$$



D/A converters

- 3 bit digital to analog (D/A) converter



$$\frac{v_{out}}{1000} + \frac{v_1}{4000} + \frac{v_2}{2000} + \frac{v_3}{1000} = 0$$

$$v_{out} = -\frac{1}{4}[v_1 + 2v_2 + 4v_3]$$

When $Q_1=1$, $v_1=4v$
else $v_1=0v$

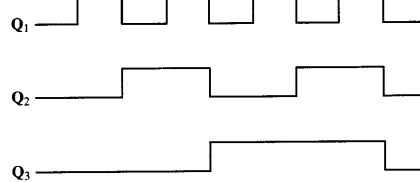
$$v_{out} = -[Q_1 + 2Q_2 + 4Q_3]$$

V_{out} is proportional to the values of $Q_1, Q_2, Q_3 \dots$

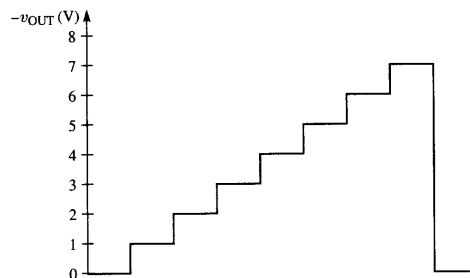
D/A converters (continue)

$$v_{out} = -[Q_1 + 2Q_2 + 4Q_3]$$

- If Q_1, Q_2, Q_3 are:

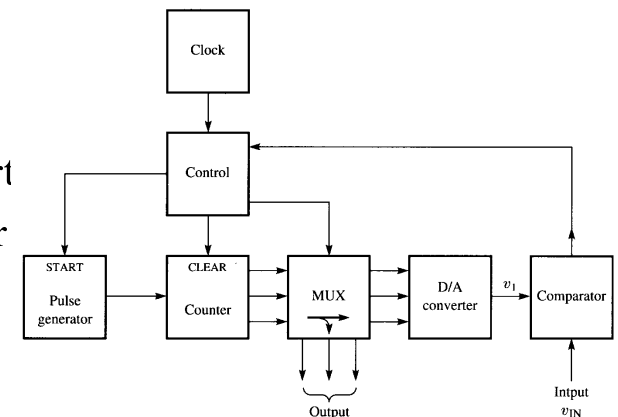


- Then V_{out} will be:



Analog to Digital (A/D) converters

- Clock
- Counter
- D/A convert
- Comparator
- Control



Percentage quantization error = $100 \times 1/(2^N - 1)$, for a N-bit system
 Example: 16 bit CD system has a quantization error of 0.001526% \equiv Signal/Noise ratio of = $20 \times \log(\text{error}) = 96.3 \text{ dB}$

A/D converters (example)

- Suppose the speed of an 8-bit A/D converter is limited by the counter, which has a maximum speed of 4×10^7 count per second. Estimate the maximum number of A/D conversions per second that can be obtained.

Maximum speed (counter) of 4×10^7 count per second

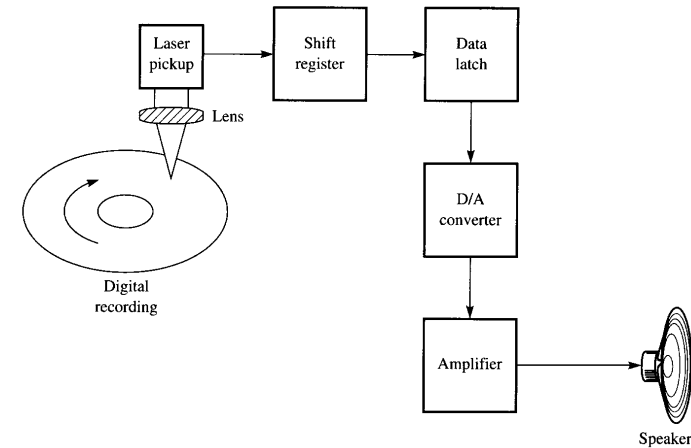
Maximum number of count per signal (worse case) is $2^8 - 1 = 255$ count

Minimum time per count = $255 / (4 \times 10^7) = 6.375 \mu\text{sec}$

Maximum number of conversion is the reciprocal of that
 $= 1 / 6.375 \mu\text{sec} = 157,000$ time per second.

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Compact Disc



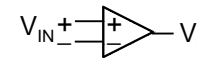
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Summary

- A register is a set of N FF, which can store N-bit of info. 4-bit bytes are conveniently represented by hexadecimal digit. A number can be represented by binary, decimal, or hexadecimal form.
- A shift register is a small system that collects bytes of data when the bits are arriving serially.
- Counters are small systems that move through a cycle of states, moving 1 step for each input.
- Usefully tool for analyzing sequential system are timing diagrams, states tables and state diagrams.
- Analog to digital and digital to analog converters are used as interfaces between analog and digital system.

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WHAT ARE I-V CHARACTERISTICS OF AN ACTUAL HIGH-GAIN DIFFERENTIAL AMPLIFIER ?

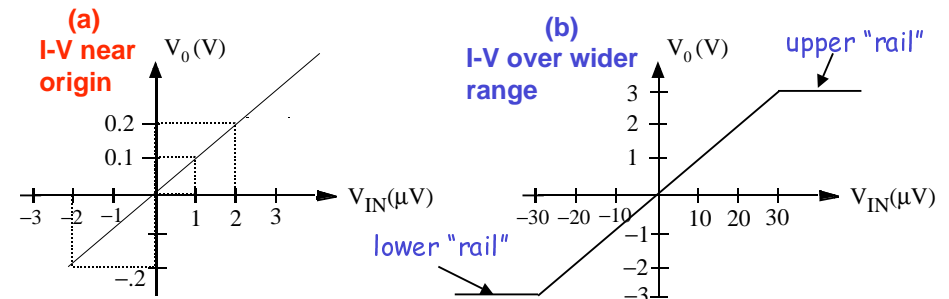


- Circuit model gives the essential linear part

- But V_0 cannot rise above some physical voltage related to the positive power supply V_{CC} ("upper rail") $V_0 < V_{+RAIL}$

- And V_0 cannot go below most negative power supply, V_{EE} i.e., limited by lower "rail" $V_0 > V_{-RAIL}$

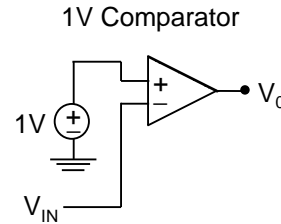
Example: Amplifier with gain of 10^5 , with max V_0 of 3V and min V_0 of -3V.



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OP-AMPS AND COMPARATORS

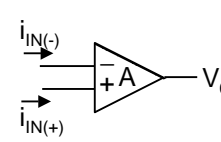
A very high-gain differential amplifier can function **either** in extremely linear fashion as a very nonlinear device – a comparator.



Open loop or Positive Feedback: Comparator

EASY WAY TO GET ANSWER FOR OP-AMP CIRCUITS

“Ideal Op-Amp Technique”:



(1) $V_+ \equiv V_-$

Why? V_0 CANNOT $\rightarrow \infty$, BUT $A \rightarrow \infty \Rightarrow V_+ \rightarrow V_-$ in order that $V_0 = A(V_+ - V_-)$
 Finite \rightarrow infinite \rightarrow must be zero

(2) $i_{IN+} \approx 0$
 $i_{IN-} \approx 0$

Why? (a) R_{IN} large by design
 (b) $V_+ \rightarrow V_- \Rightarrow$ voltage difference across $R_{IN} \rightarrow 0$

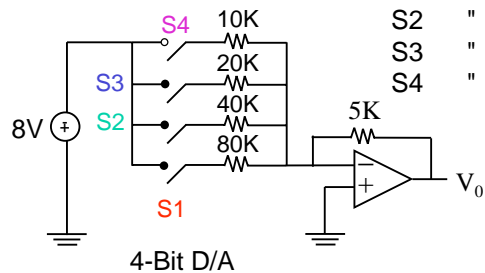
With ideal op-amp technique we can analyze all sorts of **negative feedback** circuits

- Examples: (1) unity gain follower
 (2) amplifiers
 (3) summing amplifiers

MULTI-BIT A/D AND D/A CONVERSION

Example: Digital representation of sound to analog (so you can hear it!) \rightarrow D/A conversion

The summing junction op-amp provides a simple means of D/A conversion via **weighted-adder D/A converter**



- S1 closed if LSB = 1
- S2 " if next bit = 1
- S3 " if " " = 1
- S4 " if MSB = 1

Binary number	Analog output (volts)
0 0 0 0	0
0 0 0 1	.5
0 0 1 0	1
0 0 1 1	1.5
0 1 0 0	2
0 1 0 1	2.5
0 1 1 0	3
0 1 1 1	3.5
1 0 0 0	4
1 0 0 1	4.5
1 0 1 0	5
1 0 1 1	5.5
1 1 0 0	6
1 1 0 1	6.5
1 1 1 0	7
1 1 1 1	7.5

\uparrow MSB \uparrow LSB 23

Another circuit to do this is shown in reader (R-2R resistive ladder D/A converter)

Yet another way (not shown) is to sum **charges** instead of current with capacitor networks