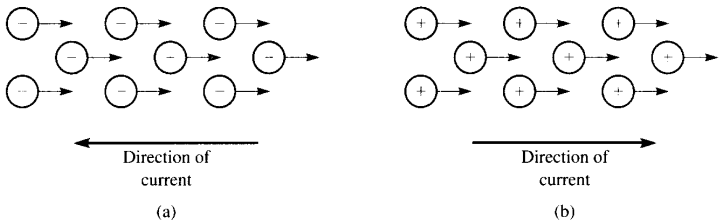
Transistors/Transistors switches/DTL/TTL

Today: (13.3, 15.1, 15.2)

- Bipolar Transistor (npn and pnp)
- Transistor switches
- DTL and TTL Logic Circuits

Semiconductors

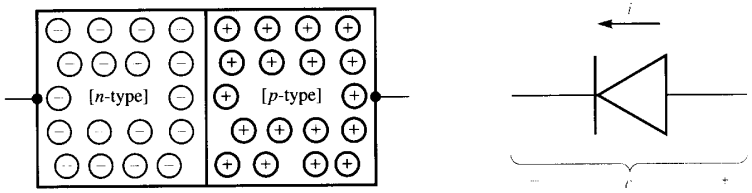
- Materials - silicon crystal
- Electrical conduction in semiconductors can take place when negative charged electrons or positive charged holes (absent of electrons) move through the crystal.



- Material contain primarily free electrons is known as n-type semiconductor
- Material contain primarily holes is known as p-type semiconductor

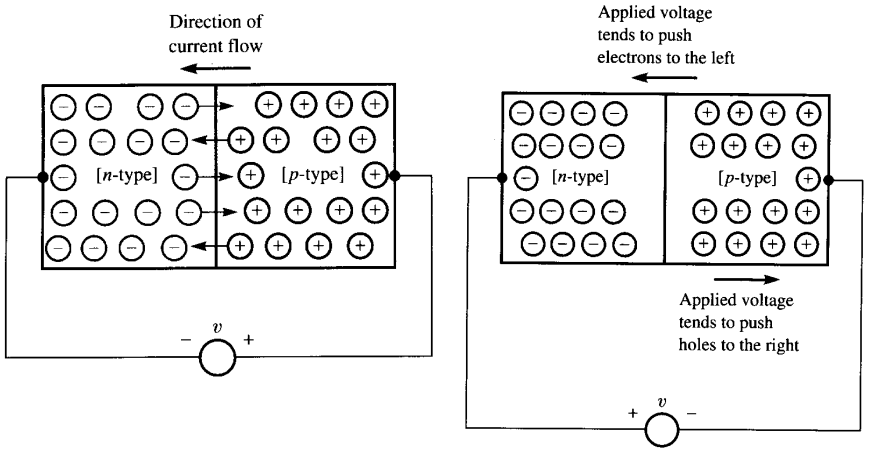
Diodes

- When p-type and n-type materials are placed in contact, the result structure is called pn junction.



- In p-type material, holes are the majority carriers, electrons are minority carriers.
- In n-type material, electron are the majority carriers, holes are minority carriers.
- Three phenomena: (1) one way conduction; (2) injection of
- minority carriers when forward biased; (3) collection of
- minority carriers when zero or reverse biased.

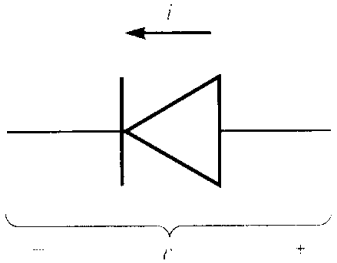
Forward Bias/Reverse Bias



I-V characteristic of pn junction

- Ideal pn junction obeys the equation

$$i = I_s\left(e^{qv/kT} - 1\right)$$



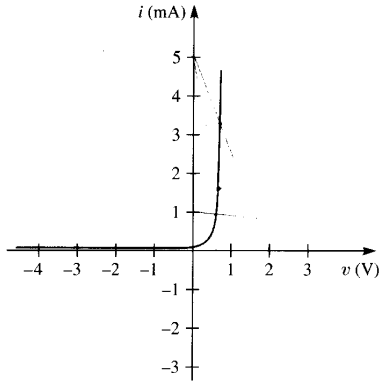
Where i and v are defined as shown in the diagram on the right
q is the electronic charge,
k is Boltzmann's constant
T is temperature in degree Kelvin
kT/q has a dimension of voltage, Vto (thermal voltage) =kT/q
Vto (300K or room temperature) is 0.026V.
I_s is saturation current constant (but depends on the size of the junction, impurity concentration, and temperature)

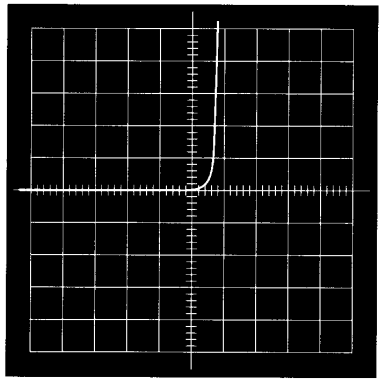
I-V characteristic of pn junctions

$$i = I_s\left(e^{qv/kT} - 1\right)$$

With $I_s = 10^{-13}$A

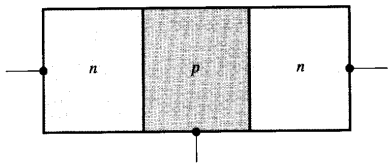
Vertical scale: 1mA per large division
Horizontal scale: 1V per large division



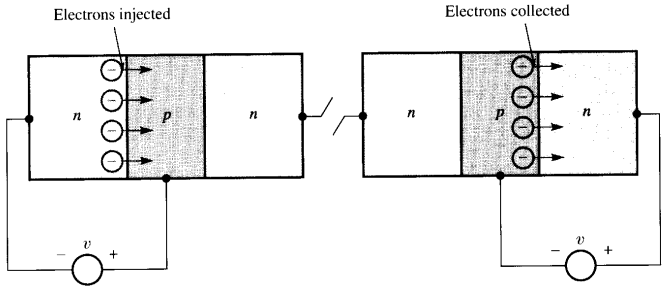


Bipolar Transistor (npn/pnp transistors)

Two pn junctions make a npn transistor

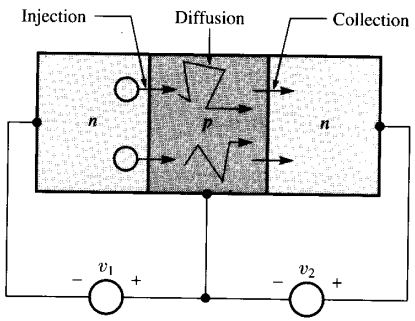


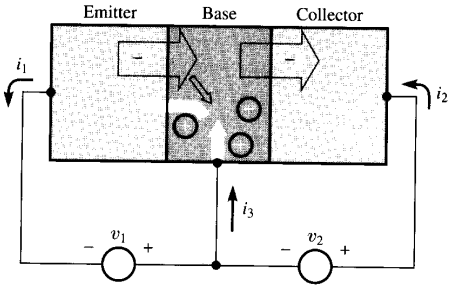
Emitter Base Collector



Forward bias Reverse bias

Bipolar transistors (npn)





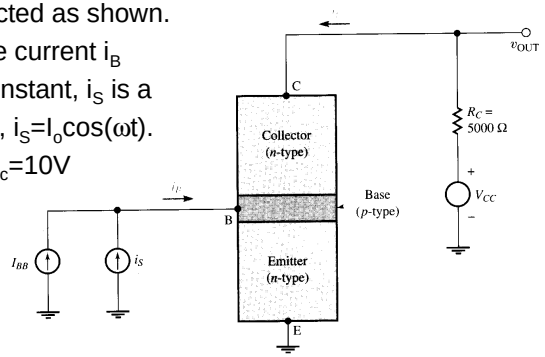
$$i_1 \approx i_2, i_1 >> i_3$$

Most emitter electrons flow into the collector (emitter current i_1 and collector current i_2 are approx. the same) and small amount flow out of the base as i_3.

Example

- A bipolar transistor is connected as shown.

Assume ic is related to the base current i_B according to $i_C = 100 i_B$. I_{BB} is constant, i_S is a small time varying input current, $i_S = I_o \cos(\omega t)$. Find v_{out} if $I_{BB}=10\mu A$, $I_o=4\mu A$, $V_{cc}=10V$



Based on Ohm's law:

$$v_{out} = V_{CC} - R_C i_C = V_{CC} - R_C(100 i_B)$$

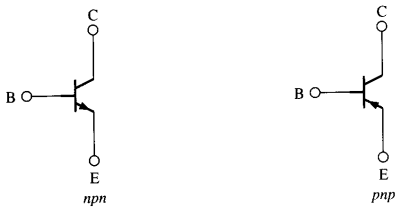
$$v_{out} = V_{CC} - R_C 100(I_{BB} + i_S)$$

$$v_{out} = V_{CC} - (5000)100(10\times10^{-6} + 4\times10^{-6}\cos\omega t)$$

$$v_{out} = 5 - 2\cos(\omega t) V$$

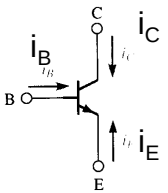
Conventions & symbols

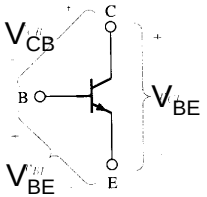
The arrow indicates the direction of the current flow.



By KCL:

$$i_E + i_B + i_C = 0$$



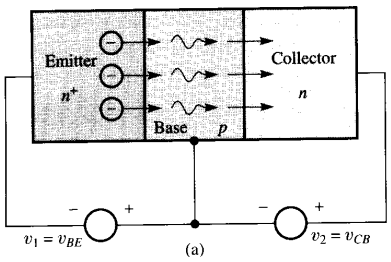


By KVL:

$$V_{EB} + V_{BC} + V_{CE} = 0$$

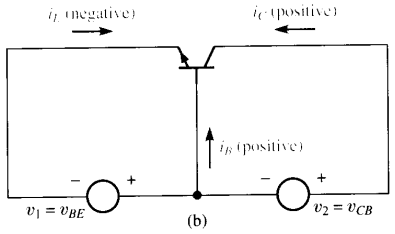
Bipolar transistor in active mode

Active mode of transistor means emitter injects electrons into the base--base-emitter (pn junction) is forward biased.



V_{BE} must be sufficiently positive to make the sufficient current flow in the base-emitter junction.

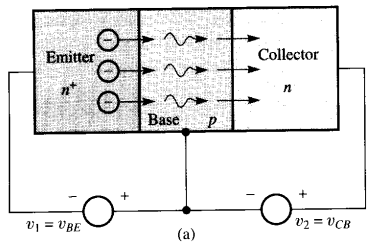
Most electrons injects by the emitter are collected by the collector, the fraction are defined as α. $i_C = -\alpha i_E$



(-ve sign because the actual i_E is going the opposite direction)

(npn transistor biased in active mode)

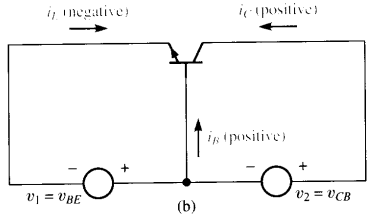
The circuit showing a appropriate polarity for active mode operation.



Another relationship:

$$i_C = \beta i_B$$

where $\beta = \dfrac{\alpha}{1-\alpha}$



Typically, $\left.\begin{matrix}\alpha \approx 1 \\ 50 < \beta < 1000\end{matrix}\right\}$ (when transistors are in active mode)

(Continue)

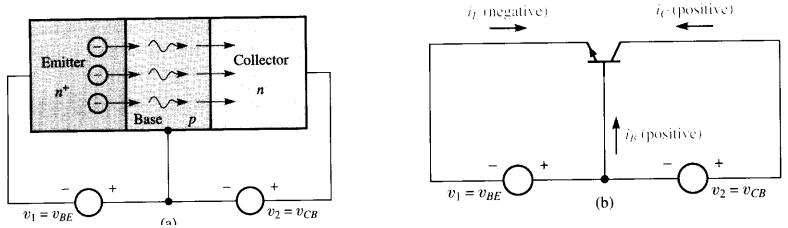
In active mode, base-emitter junction acts like a forward biased pn junction

$$i_E = -I_{ES}\left(e^{qv_{BE}/kT} - 1\right) \approx -I_{ES}\left(e^{qv_{BE}/kT}\right)$$

I_{ES} is a constant determined by the design of the transistor.
-1 is dropped because at active mode, exp(qV/kT) >>1.

Any small change in V_{BE} can lead to large change in i_E and i_C. (e.g. For active mode, V_{BE} is changed by 0.018V, i_E *is doubled.*

Bias polarities for transistors operating in active modes

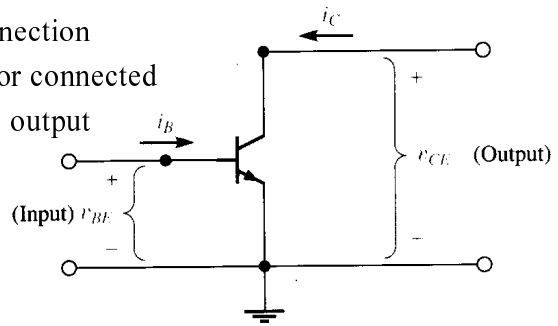


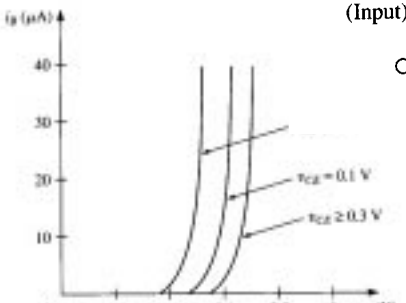
(polarity)

Parameters	npn	pnp
V_{CE}	positive	negative
V_{BE}	positive	negative
V_{CB}	positive	negative
i_E	negative	positive
i_B	positive	negative
i_C	positive	negative

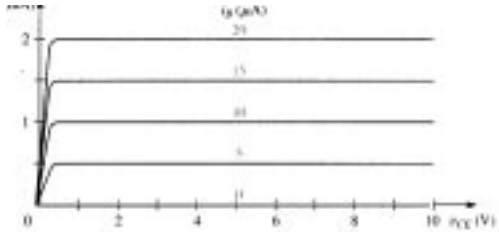
Graphical Characteristics

- Common emitter connection (the emitter is common or connected to both the input and the output ports)



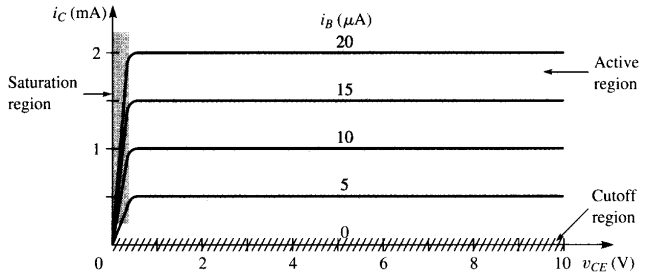


Input characteristic of a npn silicon transistor in common emitter configuration.



Output characteristic of a npn transistor in the common emitter configuration.

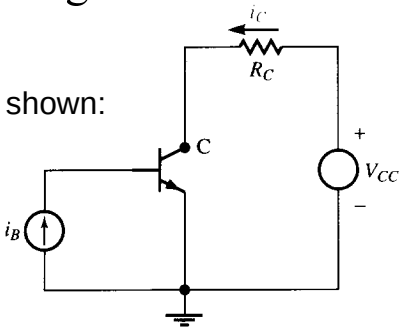
Active, Saturation, Cutoff regions



Active region: V_{CE}>0.7V, i_C is independent of V_{CE}
Cutoff region: $i_B = 0$, i_C is small.
Saturation region: Typically when V_{CE} is less than 0.7V. Low value of V_{CE} means that the collector base junction has lost its reverse bias -- the collector lost its ability to collect electrons, i_C becomes less than βi_B. (undesirable in amplifier, but useful in digital circuits)

Saturation region

- How saturation comes?
- Applies Ohm's law to the ckt as shown:



$$v_{CE} = v_{CC} - i_C R_C$$

In active mode, $i_C = \beta i_B$

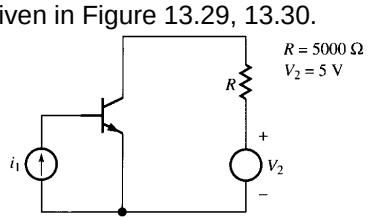
$$v_{CE} = v_{CC} - \beta i_B R_C$$

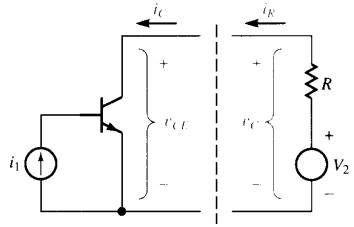
As we increase i_B, V_{CE} decreases, eventually approach 0.7V. Collector junction lost its reverse bias and the transistor enter saturation mode. Any increase in i_B does not result in proportional increase in i_C ($i_C \neq \beta i_B$). V_{CE} decreases to a minimum value of approximately 0.2V.

In Saturation mode: (1) $i_B > i_C/\beta$ (2) $V_{CE} = V_{CE}(Sat) \approx 0.2V$

Example

Find the collector current of the transistor for the following 3 values of i_1: 0, 5, and 20μA, Assume the transistor is a "typical" transistor who's characteristic is given in Figure 13.29, 13.30.





Use graphical load-line method. Assume a imaginary break is made in the circuit as shown in the right.

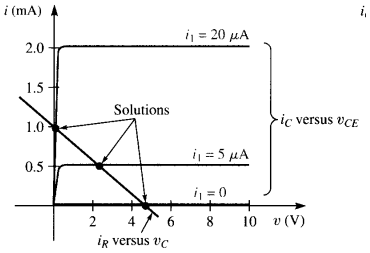
From KVL: $v_C = V_2 - i_R R$

Solutions:

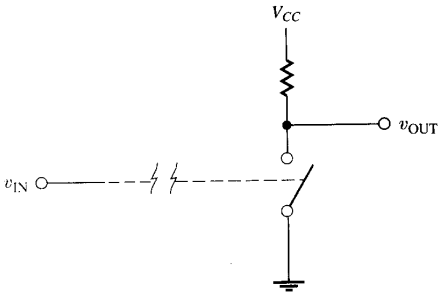
V_C=5V, i_1=0μA, i_C=0mA (cutoff)

V_C=2.5V, i_1=5μA,i_C=i_R, i_C=0.5mA (active region)

V_C=0.25V=V_{CE}, i_1=20μA, i_C=0.95mA (Saturation region)

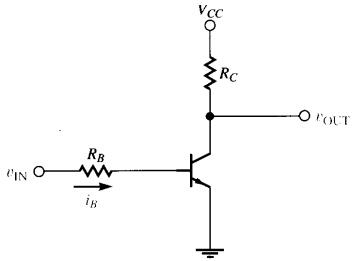


Digital Circuits/Transistor Switches



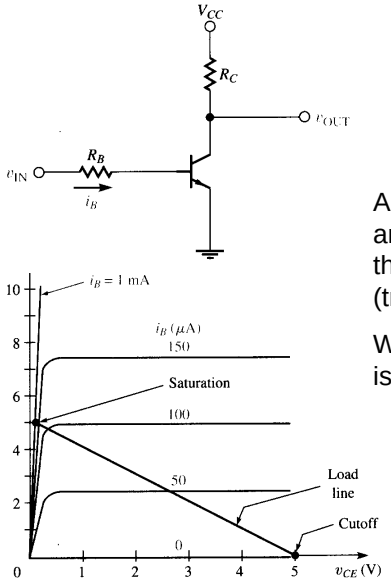
Mode of transistor switch. The position of the switch is determined by whether V_{in} is "low" or "high".

For a inverter circuit, a "low" V_{in} will disconnect the switch. (V_{out}=V_{cc})



Assume high range is 4-5V.
Low range is 0-0.5V. V_{CC}=5V

Bipolar transistor inverter



Assume high range is 4-5V.
Low range is 0-0.5V. V_{CC}=5V

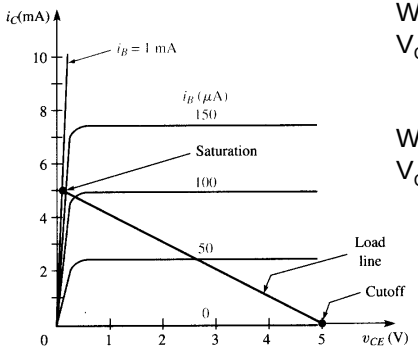
Assume R_B=1kΩ, with V_{IN} = low, results in an operating point where the load line meet the characteristic corresponding to i_B=0. (transistor in cutoff)

When V_{IN} = high, the base-emitter junction is forward biased.

$$i_B = \frac{V_{IN} - 0.7}{R_B}$$

Assume i_B = 1mA, average high voltage is 4.5V ⇒ R_B=3.8kΩ

(continue)



When V_{in} is low (V_{in} < 0.5V)
V_{CE} = High (5V, **transistor in cutoff**)

When V_{in} is high (4< V_{in} < 5V)
V_{CE} = low (0.2V, **transistor in saturation**)

Notice V_{CE} is independent of i_B. Whether i_B equals 150μA or 1mA still gives approximately V_{CE} = 0.2V)

When the input to the inverter in "high", it is important that the base current be large enough to drive the transistor to saturation.

For saturation, $i_B > i_C/\beta$, $$i_C = \frac{V_{CC} - V_{OUT}}{R_C}, V_{OUT} = V_{CE}$$

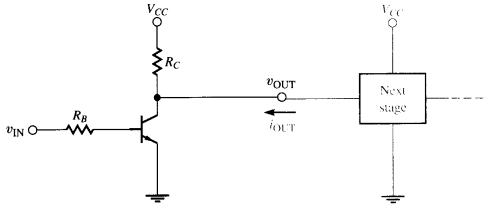
(Continue)

$$i_B > \frac{i_C}{\beta} = \frac{V_{CC} - V_{CE}}{\beta R_C}$$

$V_{CE} = V_{CE\,(SAT)}$

$$i_B > \frac{i_C}{\beta} = \frac{V_{CC} - V_{CE(SAT)}}{\beta R_C}$$

Multiple Stages Digital Circuits (loaded circuit)



Until now, we have been ignoring the current coming from the next stage. (no load effect until now)

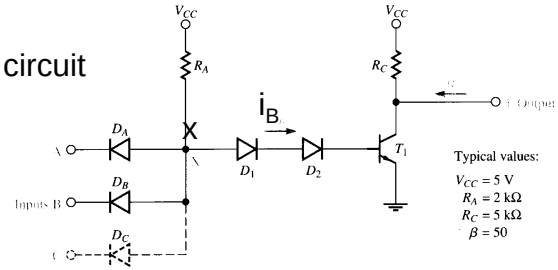
In the circuit above, when V_{out} is "low", i_{out} will normally be positive. Since i_{out} is not zero, we need to take it into account in our load calculation. By KCL:

$$i_C = \frac{V_{CC} - V_{CE(SAT)}}{\beta R_C} + i_{OUT} \quad \Rightarrow \quad i_B > \frac{i_C}{\beta} = \frac{V_{CC} - V_{CE(SAT)}}{\beta R_C} + \frac{i_{OUT}}{\beta}$$

∴ Larger i_B must be supplied when load currents are expected.

DTL (Diode Transistor Logic Circuits)

NAND DTL circuit



To simplify the analysis, we will approx. the voltage of a forward biased pn junction to be 0.7V.

Since we don't know which diode is forward bias/reverse bias, let's start by guessing the result, then check for consistency.

Let v_A and v_B = 0V, D_A and D_B are forward biased⇒ V_x=0.7V

Since it takes V_x to be 2.1V to turns on D_1, D_2, and T_1 ⇒ D_1, D_2, and T_1 are cutoff ⇒ i_B=0. ⇒V_{output}=V_{CC}=5V. D_A, D_B on, D_1, D_2, and T_1 off, consistency check out ok.

DTL NAND gate summary

Output corresponding to the various inputs for the DTL NAND gate.

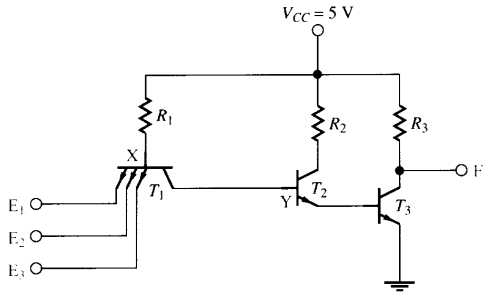
			Conduction?			
v_A	v_B	v_X	D_A	D_B	$D_1D_2T_1$	v_F
0	0	0.7	Yes	Yes	No	5
0	0.3	0.7	Yes	No	No	5
0.2	4.5	0.9	Yes	No	No	5
4.8	4.1	2.1	No	No	Yes	0.2

NAND truth table

v_A	v_B	v_F
Low	Low	High
Low	High	High
High	Low	High
High	High	Low

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

TTL (Transistor Transistor Logic Circuits)



2 inputs connect to high, 1 input to low.

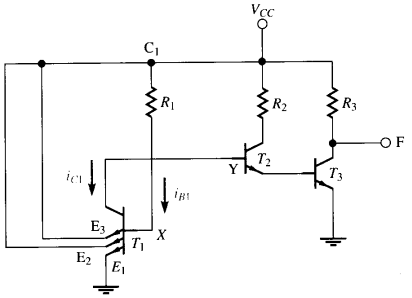
TTL NAND gate (different cases)

Case 1: one or more input are “low”, output is high.

E_1 is connected to low, E_2 and E_3 are connected to high.

Since E_1 is connected to low T_1 is on, V_x = 0.7V,

$$i_{B1} \cong (V_{CC} - 0.7)/R_1$$



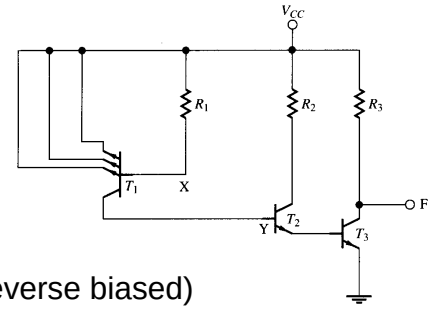
Notice that i_{C1} is flowing into T_1 and flowing from the base of T_2. This means T_2 (npn) is reverse biased. Since reverse bias current are small, $i_{B1} >> i_{C1}/\beta \Rightarrow$ T_1 is saturated $\Rightarrow V_{CE1}=V_{CE(SAT)} \cong 0.2V$. $\Rightarrow V_Y \cong 0.2V$ (T_2 and T_3 are performing the same function as D_1, D_2, T_1 in DTL) V_Y is smaller than 1.4V, the required voltage to activate T_2 and $T_3 \Rightarrow$ T_2 and T_3 are turn off $\Rightarrow V_F = V_{CC}$.

$\therefore$ one or more input are “low”, output is high.

TTL NAND gate (different cases continue)

Case 2: All inputs are “high”, output is low.

E_1, E_2 and E_3 are connected to high.



If T_1 were forward biased, $V_x = 0.7V+V_{CC}$ But V_x can not be higher than V_{CC}.
There is current flowing from V_{CC} thru R_1 into the base of T_1(reverse biased) into the base of T_2 and T_3.
V_X=2.1V, V_Y=1.4V, T_3 is saturated (because the emitter of T_2 is driving the base of T_3) $\Rightarrow V_{out}$ = low.

Summary

- Fundamental circuit of digital logic is the transistor switch, or inverter.
- Saturating bipolar transistor switches are used in diode-transistor logic (DTL) and transistor-transistor logic (TTL). The transistor acts as a switch that connects or disconnect the collector and the emitter. The switch is closed when sufficient base current is applied to saturate the transistor.
- Sufficient base current must be applied to BJT inverters to guarantee saturation under all load conditions.
- Logic family in different forms known as logic families.
- Blocks in the same family are compatible and can be interconnected.
- The TTL family and CMOS/BiCMOS family are the frequent used logic families.