EECS 42 – Introduction to Electronics for Computer Science

Spring 2003, Prof. A. R. Neureuther
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Course Web Site http://www-inst.EECS.Berkeley.EDU/~ee42/

Topical Coverage Second Midterm

Midterm Wednesday April 16th In class,
Closed book, EE42 Device Models provided,
Bring a calculator, paper provided
Review Session 5:30-7:00 PM, Monday, April 14th, 241 Cory

Schwarz and Oldham Material followed by skills

Chapter 2: all except 2.4 Loop Analysis, 2.6 and 2.7, light on 2.5
- Node analysis of circuits with up to 8 branches
- Voltage and current dividers

Chapter 3: all
- Equivalent circuits: Thevenin and Norton
- Nonlinear loads and load lines

Chapter 4: all but only ideal op-amps
- Dependent sources, gain, input and out put impedance
- Ideal Op-Amps
- **Generalization to Comparators (Lecture 15)**

Chapter 5: all light on 5.3 and very limited inductor circuits.

Chapter 8.1: Only 8.1
- EE 40/42 simple solution method and application to switching and pulses
- KCL to get differential equation for capacitor voltage and inductor current

Chapter 10: no flip-flops
- Gates and logic functions
- **Generalization: Timing diagrams (Lecture 12)**

Lectures 16-17 Handouts, pp. 522-524, 604-611 Logic with state dependent devices
- Device I vs. V curves and load line method
- Simple inverter and voltage transfer function
- Complementary Pull-Up and Pull-Down networks (CMOS)

Likely Exam Emphasis

Analysis of vanilla circuits with dependent sources
Ideal Op-Amps
Analysis of circuits using dependent sources to improve characteristics
Logic Functions and Timing Diagrams
Static analysis of logic gates using **the I vs. V model for EE42**

EE 42 Device

$$I_{OUT-SAT-D} = k_D (V_{IN} - V_{TD}) V_{OUT-SAT-D}$$

$$I_{OUT-SAT-U} = k_U (V_{DD} - V_{IN} - V_{TU}) V_{OUT-SAT-U}$$

When in circuit attached to VDD.

Example Values

$k_D = 25\ \mu A/V^2$	$k_U = 20\ \mu A/V^2$
$V_{TD} = 1V$	$V_{TU} = 1V$
$V_{OUT-SAT-D} = 1V$	$V_{OUT-SAT-U} = 1V$