EECS 42 – Introduction to Electronics for Computer Science

Fall 2001, **Prof. A. R. Neureuther**
Dept. EECS, **510 Cory 642-4590**
UC Berkeley **OH last week and finals M, Tu, W, Th, F 11 (10 on 14th)**
Course Web Site http://www-inst.EECS.Berkeley.EDU/~ee42/

Final Exam,
12:30-3:30 PM Friday December 14th, F 295 Haas
Closed Book – Device Equations Provided
Bring Claculator, Paper provided
Review Session #1: 5-6:30 PM Mon. Dec 10, (2nd Floor) Cory
Review Session #2: 5-6:30 PM Wed. Dec 12, (2nd Floor) Cory

Topical Coverage for Final Exam

Chapter 2: all except 2.4 Loop Analysis, 2.6 and 2.7, light on 2.5
Node analysis of circuits with up to 8 branches, Voltage and current dividers

Chapter 3: all
Equivalent circuits: Thevenin and Norton; Nonlinear loads and load lines

Chapter 4: all but only ideal op-amps
Dependent sources, gain, input and out put impedance; Ideal Op-Amps; **Comparators**.

Chapter 5: all light on 5.3 and very limited inductor circuits.

Chapter 8.1: Only 8.1 EE 40/42 solution method; KCL to get differential equation; pulses

Chapter 10: no flip-flops Gates and logic functions; Timing diagrams

Lectures 15-19, O&S pp. 522-524, 604-611 Logic with state dependent devices
Device I vs. V curves and load line method; Simple inverter and voltage transfer function; Complementary Pull-Up and Pull-Down networks (CMOS)
Dynamic (Transient) Switched Resistor Model and 0.69RC delay; Worst case propagation delay, Cascade propagation delay, Latch to hold and synchronize, Feedback to create memory.

Lectures 20-22, O&S pp. 481-499, 511-527, 594-598, Device physics and models
Diode equation, perfect rectifier and large signal models and use in circuits.
Large signal bipolar transistor model and uses in inverter circuits.
Carrier motion as basis for conductance and conductance of MOS

Lectures 23-24 O&S pp. 604-618 and viewgraphs: CMOS Gates
Static: Logic function, Voltage Transfer Function, V_M, Resistance model, D.C. power
Dynamic: Capacitance for each source/drain and gate, which capacitors change voltage in switching, resistive path, worst-case propagation delay, Use of Latches and designing clock delay, short-circuit current, a.c. power consumption due to capacitor charging and short-circuit current.

Likely Exam Emphasis

Since 2nd Midterm	**From before 2nd Midterm**
• CMOS Static Type Analysis (big): Current given voltage, V_{OUT} vs. V_{IN}, Short Circuit Current, D.C. power • CMOS Transient Analysis (big): Sources and amount of capacitance, propagation delay, a.c. power, clocked latches • Diode and Bipolar Transistor (medium): No physics but large signal analysis • Physics (small): Resistance from carrier motion, field effect carriers and resistance **10-20 pts C, 20-30 pts B, and 40-50 pts A**	• Equivalent Circuits and Load Lines: load circuits, VTF • Dependent Sources: Gain, input and output resistance • Ideal Op-Amps • Transients • Gates: Logic function and timing diagrams **50-60 pts C, 30-40 pts B, and 10-20 pts A.**