5/12/03

EECS 42 – Introduction to Electronics for Computer Science

Spring 2003, Prof. A. R. Neureuther
Dept. EECS, 510 Cory 642-4590
UC Berkeley Office Hours During Finals: TBA See web
Course Web Site http://www-inst.EECS.Berkeley.EDU/~ee42/

Topical Coverage Final Exam

5-8 PM Tuesday, May 20 room 277 Cory
Closed Book – Device Equations Provided
Bring Calculator, Paper provided
Review Session (11-12:30), Monday, May 19th, room TBA
Office Hours: 1st week regular; (19th 2C, 3K 4N, 20th 11N, 1C, 2K)
Schwarz and Oldham Material followed by skills

Chapter 2: all except 2.4 Loop Analysis, 2.6 and 2.7, light on 2.5
Node analysis of circuits with up to 8 branches, Voltage and current dividers

Chapter 3: all
Equivalent circuits: Thevenin and Norton; Nonlinear loads and load lines

Chapter 4: all but only ideal op-amps
Dependent sources, gain, input and out put impedance; Ideal Op-Amps; **Comparators (15)**.

Chapter 5: all light on 5.3 and very limited inductor circuits.

Chapter 8.1: Only 8.1 EE 40/42 solution method; KCL to get differential equation; pulses

Chapter 10: no flip-flops Gates and logic functions; Timing diagrams (12)

Lectures 16-17, O&S pp. 522-524, 604-611 Static Logic with state dependent devices
Device I vs. V curves and load line method; Static Power
Simple inverter and voltage transfer function; Complementary Pull-Up and Pull-Down (CMOS)

Lectures 18-22 O&S pp. 604-618 and viewgraphs: Dynamic Logic
Dynamic (Transient) Switched Resistor Model and 0.69RC delay;
Worst case propagation delay, Cascade propagation delay, Dynamic Power CV^2
Use of Latches and designing clock delay

Lectures 23-24, O&S pp. 481-499, 511-527, 594-598, Device physics and models
Diode equation, perfect rectifier and large signal models and use in circuits.
Carrier motion as basis for conductance and conductance-resistance of MOS

Likely Exam Emphasis

Transient
Ideal Op-Amps, Dependent Sources, Gain, Thevenin resistance
Diode circuit analysis and signal processing
Static analysis of logic gates using the I vs. V model for EE42
CMOS Logic Functions, Delay,
Timing Diagrams, Latches

EE 42 Device

$$I_{OUT-SAT-D} = k_D\left(V_{IN} - V_{TD}\right)V_{OUT-SAT-D}$$

$$I_{OUT-SAT-U} = k_U\left(V_{DD} - V_{IN} - V_{TU}\right)V_{OUT-SAT-U}$$

When in circuit attached to VDD.

$$\sigma = qN\mu$$

Example Values
k_D = 25 μA/V² k_U = 20 μA/V²
V_{TD} = 1V V_{TU} = 1V
$V_{OUT-SAT-D}$ = 1V $V_{OUT-SAT-U}$= 1V

$$R = \frac{L}{\sigma \cdot h \cdot w} = \left(\frac{1}{\sigma \cdot h}\right)\left(\frac{L}{W}\right) = R_{SHEET}\left(\frac{L}{W}\right)$$