EECS 42 – Introduction to Electronics for Computer Science

Spring 2003 Prof. A. R. Neureuther
Dept. EECS, 510 Cory 642-4590
UC Berkeley OH M, Tu, W, (Th), F 11
Course Web Site http://www-inst.EECS.Berkeley.EDU/~ee42/

Midterm #2 April 16th, 2003

Closed Book, Closed Notes
Device Equations on Device Problem
Write on the Exam paper

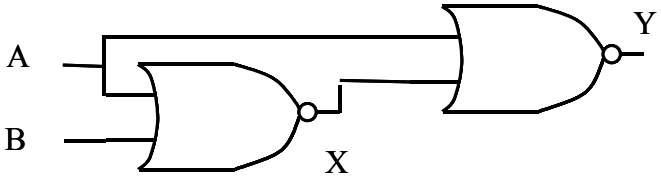
Print Your Name:____Solution_____

Sign Your Name:_____

Show your work so that the method as well as the answer can be graded for correctness and completeness. Correct answers alone are only worth 70% of full credit.

Problem	Possible	Score
I	30	
II	35	
III	35	
Total	100	

I (30 Points) Logic and Timing Diagrams

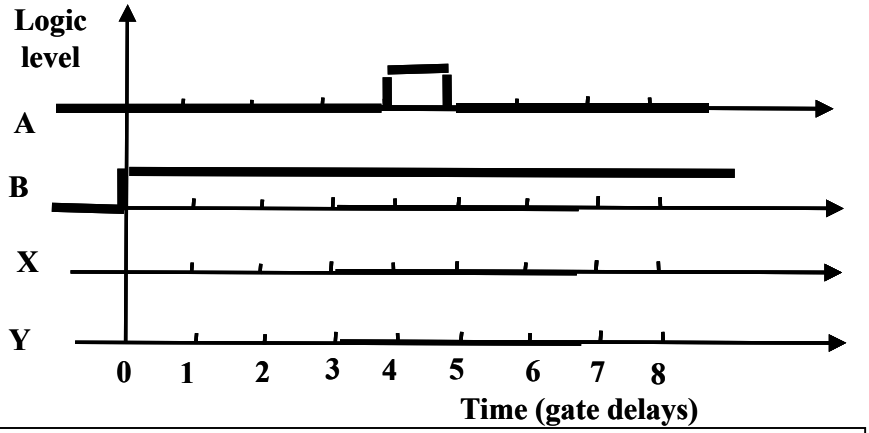


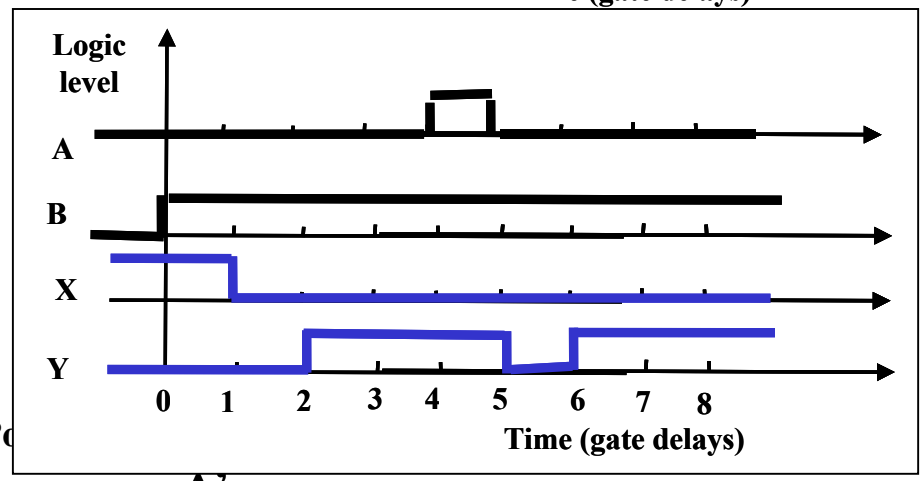
a) (12 points) Complete the truth table.

A	B	X	Y
0	0		
1	0		
0	1		
1	1		

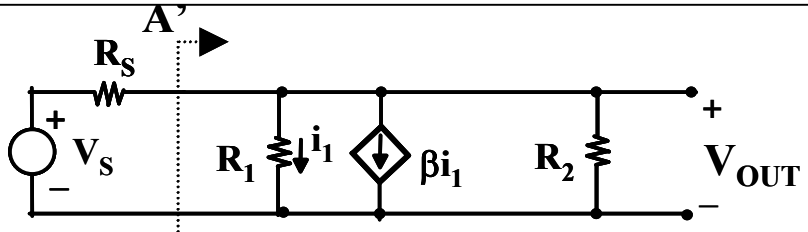
A	B	X	Y
0	0	1	0
1	0	0	0
0	1	0	1
1	1	0	0

b) (18 points) Complete the timing diagram for all eight gate delays.





II (35 Pc



a) (15 points) Find V_{OUT} in terms of V_S, the resistors and the dependent source strength β.

$$i_b = V_{OUT} / R_1$$
$$\beta i_b = \beta V_{OUT} / R_1$$
$$V_{OUT}\left(\frac{1}{R_1}+\beta\frac{1}{R_1}+\frac{1}{R_2}\right)+\frac{(V_{OUT}-V_S)}{R_S}=0$$
$$V_{OUT} = V_S \frac{\frac{1}{R_S}}{\left(\frac{1}{R_1}+\beta\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_S}\right)}$$

b) (12 points) Find the resistance seen looking to the right of AA' in terms of the resistors and the dependent source strength β.

Apply v_{TEST} to the input then find i_{TEST}

$$i_{TEST} = \frac{V_{TEST}}{R_1}+\beta\frac{V_{TEST}}{R_1}+\frac{V_{TEST}}{R_2} = V_{TEST}\left(\frac{\beta+1}{R_1}+\frac{1}{R_2}\right)$$

$$\frac{V_{TEST}}{I_{TEST}} = \frac{1}{\left(\frac{\beta+1}{R_1}+\frac{1}{R_2}\right)} = \left(\frac{R_1}{\beta+1}\right) \| R_2$$

c) (8 points) Does increasing β raise or lower the resistance in part b)? Give a brief intuitive explanation of how this occurs.

Raising β reduces the resistance as whatever current that flows into R1 is always matched by a β times larger current through the dependent source. This same current is exactly the same current that would flow through resistor R1 if it were (β+1) times smaller. (This reduction is diluted somewhat by R2 being in parallel.)

III (35 Points) Logic Circuit with a EE42 Device

$$I_{OUT-SAT-D} = k_D(V_{IN}-V_{TD})V_{OUT-SAT-D}$$

Values for this Exam

k_D = 40 μA/V^2 **k_U = 30 μA/V^2**

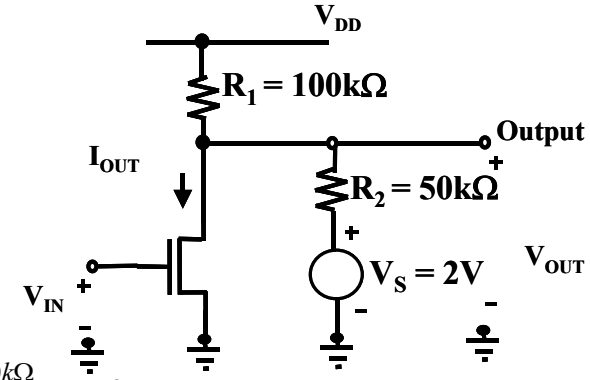
V_{TD} = 2V **V_{TU} = 1.5V**

$V_{OUT-SAT-D}$ = 0.5V **$V_{OUT-SAT-U}$= 1.5V**

$$I_{OUT-SAT-U} = k_U\left(V_{DD} - V_{IN} - V_{TU}\right)V_{OUT-SAT-U}$$

When in circuit attached to VDD.

a) (12 points) Remove the EE42 pull-down device from this circuit and consider the remaining circuit. Find the **open circuit voltage** and **short circuit current** that is seen looking out from the position of the pull-down EE42 device into the remaining circuit.



$$V_{OC} = 2V + (5V - 2V)\frac{R_2}{R_1 + R_2} = 2V + 3V\,\frac{50k\Omega}{100k\Omega + 50k\Omega} = 3V$$

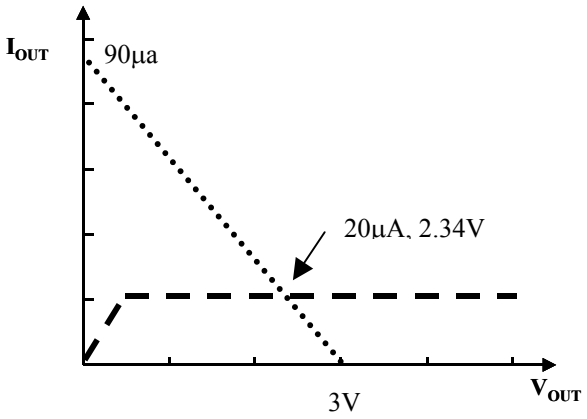
$$I_{SC\_Donward} = \frac{5V}{100k\Omega} + \frac{2V}{50k\Omega} = 50\mu A + 40\mu A = 90\mu A$$

b) (11 points) Now consider the EE 42 device alone with the parameter values given. If V_{IN} is limited to a range of 0 to 5V and V_{OUT} is limited to a range of 0 to 5V, what will be the maximum current?

Highest is when V_{IN} = 5V and V_{OUT} = 5V

$$I = \left(40\mu A/V^2\right)(5V - 2V)(0.5V) = 60\mu A$$

c) (12 points) Now consider the EE 42 device and circuit connected together. Find V_{OUT} when V_{IN} = 3V. You may use either a graphical or an algebraic method.



For V_{IN} = 3 V, ISAT = 40(3V-2V)(0.5V) = 20μA
KCL at the putput node gives

$$20\mu A = \frac{5V - V_{OUT}}{100k\Omega} + \frac{2V - V_{OUT}}{50k\Omega}$$

$$V_{OUT} = 70\mu A\,\frac{50k\Omega \cdot 100k\Omega}{50k\Omega + 100k\Omega} = 2.34V$$