Lecture # 17  Logic with Complementary Devices
S&O pp. 607-611 (read for graphs and not physics or equations), plus Handout of Wed Lectures.

A) Discovering a Pull-Up Device
B) Designing a Pull-Up Device
C) EE 42 Pull-Up Device Model (42S_PMOS)
D) Composite I_OUT vs. V_OUT
E) Voltage Transfer Function and V_MID

http://inst.EECS.Berkeley.EDU/~ee42/

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Game Plan 04/02/03

Monday 03/31/04
- Welcome back plus HW#8 coaching
- State Dependent Devices (Transistors)
- Load Line, VTC, Pull Down Device (42S_NMOS)

Wednesday 04/02/03:
- Pull-Up Device (42S_PMOS)
- VTC and V_MID

Next (11th) Week:
- Monday: 4/7/03 Logic Dynamic via Switched Resistor
- Wednesday: 4/09/03 Quiz on dependent sources; then new material on Complementary Gates

Problem set #9: Monday 3/31 and due at 2:30 4/09 in box in 240 Cory – Static Analysis of an Inverter with simplified EE 42 Device Models
Composite Current Plot for the 42S_NMOS Circuit with 200kΩ Load to Ground

- Problem #1: Current when VOUT Low
- Problem #2: Poor VOUT High with Load

Problems and Opportunities in Logic Circuit Design

Problem #1: Significant wasted current and power when VOUT is low.
Problem #2: High value of VOUT is adversely affected by a load resistor.

Missed Opportunity: The value of the input control signal is not used to adjust the state of the pull-up device.

What if: If the pull-up device could be a state-dependent device what kind of device would we want?
Pull-Up Device Design: Trial 1

Problem #1 is worse! There is even more wasted current and power than before when $V_{OUT}$ is low because both devices are on at the same time.

Look for a more Complementary approach.

Problem #1 is solved. There is essentially no wasted current or power when $V_{OUT}$ is low.

Note that in the pull-down case the current increases with the state number and in the pull-up case it decreases.
Pull-Down and Pull-Up Must Complement Rather Than Fight Each Other

Reducing the Short-Circuit Current by making either one or the other device off.

Desirable Complementary Device Characteristics

We desire characteristics that are complementary for the pull-down and pull-up state-dependent devices.

<table>
<thead>
<tr>
<th>$V_{IN}$</th>
<th>Low</th>
<th>High</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pull-Down Current</td>
<td>Low not leak</td>
<td>High Discharge Output</td>
</tr>
<tr>
<td>Pull-Up Current</td>
<td>High Charge Output</td>
<td>Low not leak</td>
</tr>
</tbody>
</table>
Designing the Complementary Device

The curve sets are very similar but have two key changes.

The creation of current with input State ($V_{IN}$) is reverse ordered (and also shifted).

The dependence on $V_{OUT}$ is reverse ordered and shifted by $V_{DD}$.

$V_{DD}-V_X$ Gives Complementary Characteristics

Physical Interpretation as device related rather than logic circuit related voltages.
Saturation Current NMOS Model

Current $I_{OUT}$ only flows when $V_{IN}$ is larger than the threshold value $V_{TD}$ and the current is proportional to $V_{OUT}$ up to $V_{OUT-SAT-D}$ where it reaches the saturation current

$$I_{OUT-SAT-D} = k_D (V_{IN} - V_{TD}) V_{OUT-SAT-D}$$

Note that we have added an extra parameter to distinguish between threshold ($V_{TD}$) and saturation ($V_{OUT-SAT-D}$).

Example:
- $k_D = 25 \mu A/V^2$
- $V_{TD} = 1V$
- $V_{OUT-SAT-D} = 1V$

$$I_{OUT-SAT-D} = 25 \mu A/V^2 (3V - 1V) V = 50 \mu A$$

Use these values in the homework.

Saturation Current 42S_PMOS Model

Current $I_{OUT}$ only flows when $V_{IN}$ is smaller than $V_{DD}$ minus the threshold value $V_{TU}$ and the current is proportional to $(V_{DD} - V_{OUT})$ up to $(V_{DD} - V_{OUT-SAT-U})$ where it reaches the saturation current

$$I_{OUT-SAT-U} = k_U (V_{DD} - V_{IN} - V_{TU}) V_{OUT-SAT-U}$$

Example:
- $k_U = 20 \mu A/V^2$
- $V_{TU} = 1V$
- $V_{OUT-SAT-U}= 1V$

$$I_{OUT-SAT-U} = 20 \mu A/V^2 (5V - 3V - 1V) V = 20 \mu A$$

Use these values in the homework.
### Transistor Inverter Example

It may be simpler to just think of PMOS and NMOS transistors instead of a general 3 terminal pull-up or pull-down devices or networks.

![Transistor Inverter Example Diagram](image-url)
Case #1: \( V_{\text{IN}} = V_{\text{DD}} = 5\text{V} \)

The Output is Pulled-Down

- The PMOS transistor is OFF when \( V_{\text{IN}} > V_{\text{DD}} - V_{\text{TU}} \)
- The NMOS transistor is ON when \( V_{\text{IN}} > V_{\text{TD}} \)

Case #2: \( V_{\text{IN}} = 0 \)

The Output is Pulled-Up

- The PMOS transistor is ON when \( V_{\text{IN}} < V_{\text{DD}} - V_{\text{TU}} \)
- The NMOS transistor is OFF when \( V_{\text{IN}} < V_{\text{TD}} \)
Composite $I_{OUT}$ vs. $V_{OUT}$ for CMOS

- PU current is flat (saturated) below $V_{DD} - V_{OUT-SAT-D}$
- PD current is flat (saturated) beyond $V_{OUT-SAT-D}$
- Pull-Up PMOS $I_{OUT-SAT-U}$
- Pull-Down NMOS $I_{OUT-SAT-D}$
- The maximum voltage is $V_{DD}$

Solution

Composite $I_{OUT}$ vs. $V_{OUT}$ to Find Points That Satisfies Both Devices for Each $V_{IN}$

- Solution Points

$V_{IN} = 0$
$V_{IN} = 3$
$V_{IN} = 5$

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Voltage Transfer Function for the Complementary Logic Circuit

State 1 for \( V_{IN} = 1V \)

State 3 for \( V_{IN} = 3V \)

State 5 for \( V_{IN} = 5V \)

VM

VM

Vertical section due to zero slope of \( I_{OUT} \) vs. \( V_{OUT} \) in the saturation region of both devices.

Method for Finding \( V_M \)

At \( V_M \),

1) \( V_{OUT} = V_{IN} = V_M \)

2) Both devices are in saturation

3) \( I_{OUT-SAT-D} = I_{OUT-SAT-U} \)

\[
I_{OUT-SAT-D} = k_D (V_{IN} - V_{TD}) V_{OUT-SAT-D}
\]

\[
= I_{OUT-SAT-U} = k_U (V_{DD} - V_{IN}) V_{TU} V_{OUT-SAT-U}
\]

Substitute \( V_M \)

Solve for \( V_M \)

Example Result: When \( k_D = k_P \), \( V_{OUT-SAT-D} = V_{OUT-SAT-U} \)

and \( V_{TD} = V_{TU} \), then \( V_M = V_{DD}/2 \)