Lecture 17: Logic with Complementary Devices

A) Discovering a Pull-Up Device

B) Designing a Pull-Up Device

C) EE42 Pull-Up Device Model (42S_PMOS)

D) Composite I_{OUT} Vs. V_{OUT}

E) Voltage Transfer Function and V_{MID}

http://inst.EECS.Berkeley.EDU/~ee42/

Problems and Opportunities in Logic Circuit Design

Problem #1: Significant wasted current and power when V_{OUT} is low.

Problem #2: High value of V_{OUT} is adversely affected by a load resistor.

Missed Opportunity: The value of the input control signal is not used to adjust the state of the pull-up device.

What if: If the pull-up device could be a state-dependent device, what kind of device would we want?

Game Plan 04/02/03

Monday 03/31/04

Welcome back plus HW#8 coaching

State Dependent Devices (Transistors)

Load Line, VTC, Pull Down Device (42S_NMOS)

Wednesday 04/02/03:

Pull-Up Device (42S_PMOS)

VTC and V_{GO}

Next (11th) Week:

Monday: 4/7/03 Logic Dynamic via Switched Resistor

Wednesday: 4/09/03 Quiz on dependent sources; then new material on Complementary Gates

Problem set #9: Monday 3/31 and due at 2:30 4/09 in box in 240 Cory – Static Analysis of an Inverter with simplified EE 42 Device Models

Composite Current Plot for the 42S_NMOS Circuit with 200kΩ Load to Ground

Problem #1: Current when V_{OUT} Low

Problem #2: Poor V_{OUT} High with Load

Pull-Up Device Design: Trial 1

Similar pull-up and pull-down states

Problem #1 is worse!

There is even more wasted current and power than before when V_{OUT} is low because both devices are on at the same time.

Look for a more Complementary approach.

Problem #1 is solved.

There is essentially no wasted current or power when V_{OUT} is low.

Note that in the pull-down case the current increases with the state number and in the pull-up case it decreases.

Problem #1 is solved. There is essentially no wasted current or power when V_{OUT} is low.
Input for State
Control Signal
Share Same Signal
Input for State
Control Signal

Desirable Complementary Device Characteristics

<table>
<thead>
<tr>
<th>$V_{IN}$</th>
<th>Low</th>
<th>High</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pull-Down Current</td>
<td>Low not leak</td>
<td>High Discharge Output</td>
</tr>
<tr>
<td>Pull-Up Current</td>
<td>High Charge Output</td>
<td>Low not leak</td>
</tr>
</tbody>
</table>

We desire characteristics that are complementary for the pull-down and pull-up state-dependent devices.

Saturation Current NMOS Model

Current $I_{OUT}$ only flows when $V_{IN}$ is larger than the threshold value $V_{TD}$ and the current is proportional to $V_{OUT}$ up to $V_{OUT-SAT-D}$ where it reaches the saturation current

$$I_{OUT-SAT-D} = k_D(V_{IN} - V_{TD})V_{OUT-SAT-D}$$

Note that we have added an extra parameter to distinguish between threshold ($V_{TD}$) and saturation ($V_{OUT-SAT-D}$). Example:

- $k_D = 25 \mu A/V^2$
- $V_{TD} = 1V$
- $V_{OUT-SAT-D} = 1V$

Use these values in the homework.

$$I_{OUT-SAT-D} = \frac{25}{V^2}[(V' - V_{TD})]V_{OUT-SAT-D}$$

Use these values in the homework.

Saturation Current 42S_PMOS Model

Current $I_{OUT}$ only flows when $V_{IN}$ is smaller than $V_{DD}$ minus the threshold value $V_{TU}$ and the current is proportional to $V_{OUT}$ up to $V_{OUT-SAT-U}$ where it reaches the saturation current

$$I_{OUT-SAT-U} = k_U(V_{DD} - V_{IN} - V_{TU})V_{OUT-SAT-U}$$

Example:

- $k_U = 20 \mu A/V^2$
- $V_{TU} = 1V$
- $V_{OUT-SAT-U} = 1V$

Use these values in the homework.

$$I_{OUT-SAT-U} = \frac{20 \mu A}{V^2}([V' - V_{DD} - V_{TU}]V_{OUT-SAT-U})$$

Use these values in the homework.
42S_PMOS Pull-Up Device Curves

I<sub>OUT</sub> vs. V<sub>OUT</sub>

Evaluating the point where V<sub>OUT</sub> = V<sub>DD</sub> - V<sub>TH</sub> for a given V<sub>IN</sub> allows the entire curve to be sketched.

Transistor Inverter Example

It may be simpler to just think of PMOS and NMOS transistors instead of a general 3 terminal pull-up or pull-down devices or networks.

Case #1: V<sub>IN</sub> = V<sub>DD</sub> = 5V

The Output is Pulled-Down

Case #2: V<sub>IN</sub> = 0

The Output is Pulled-Up

Composite I<sub>OUT</sub> vs. V<sub>OUT</sub> for CMOS

The maximum voltage is V<sub>DD</sub>

Solution

Composite I<sub>OUT</sub> vs. V<sub>OUT</sub> to Find Points That Satisfies Both Devices for Each V<sub>IN</sub>

Solution Points

V<sub>IN</sub> = 5 ± 3

V<sub>IN</sub> = 0

V<sub>IN</sub> = 3

V<sub>IN</sub> = 3 ± 2

V<sub>IN</sub> = 5

V<sub>IN</sub> = 0

V<sub>IN</sub> = 3

V<sub>IN</sub> = 3 ± 2
### Voltage Transfer Function for the Complementary Logic Circuit

- **State 1 for** $V_{IN} = 1V$
- **State 3 for** $V_{IN} = 3V$
- **State 5 for** $V_{IN} = 5V$

- $V_{OUT} = V_{IN}$

Vertical section due to zero slope of $I_{OUT}$ vs. $V_{OUT}$ in the saturation region of both devices.

### Method for Finding $V_M$

1. $V_{OUT} = V_{IN} = V_M$
2. Both devices are in saturation
3. $I_{OUT-SAT-D} = I_{OUT-SAT-U}$

$$I_{OUT-SAT-D} = k_D (V_{TD} - V_{OUT-SAT-D})$$
$$I_{OUT-SAT-U} = k_U (V_{TU} - V_{OUT-SAT-U})$$

Substitute $V_M$

Solve for $V_M$

Example Result: When $k_D = k_U$, $V_{OUT-SAT-D} = V_{OUT-SAT-U}$ and $V_{TD} = V_{TU}$, then $V_M = V_{DD}/2$