Lecture # 24 Current Flow in Silicon and N-MOS Devices

Handout of Wednesday Lecture.
A) Physics of current flow, resistance, resistivity
B) Charge transport in a sheet and velocity saturation
C) N-MOS Device Structure and Voltage Control
D) N-MOS I vs. V at low and high drain voltage

Reading: Schwarz and Oldham, pp. 518-526
http://inst.EECS.Berkeley.EDU/~ee42/

Physics of Current Flow, Resistance, Resistivity
A voltage V applied across the length L of a homogeneous material produces an electric field E where E = V/L.

A current I flows where I = V/R, and the resistance R is given by the resistor formula R = pL/A in which the resistivity, \( \rho \), is inversely proportional to the concentration of free carriers, N, and the mobility of those carriers, \( \mu \). (In fact \( \rho = 1/\sigma \), where the conductivity, \( \sigma \), is defined by \( \sigma \mu N \), in which \( q \) is the electronic charge (\( 1.6 \times 10^{-19} \) Coulomb).

Example: 1 \( \mu \) thick n-type silicon layer which was implanted with 10^{12} donors cm^{-2}. (Thus \( N_d = 10^{12} / 10^4 = 10^8 \) cm^{-2})

\( \sigma = q n \mu_R = (1.6 \times 10^{-19} \) C) \times (1000 cm^2 / Vsec) = 1.6 S/cm

\( \rho = 1/\sigma = 0.625 \Omega \) cm

Sheet resistivity, R given by:

\[ R = \frac{1}{\sigma} \frac{t}{L} = 6.25 \frac{\Omega}{\text{square}} \]

But this can be obtained directly from the implant "Q" of 1.6 \( \times 10^{10} \) (in 1.6 \( \times 10^{10} \) thus

\[ R = \frac{1}{(Q \mu)} = 6.25 \frac{\Omega}{\text{square}} \]

\[ R_{AB} = ? \]

\[ R_{AB} = 4 \times 6.25 = 25 \Omega \]
Charge Transport in Silicon

At low electric fields, the average speed of carriers is proportional to the field with proportionality constant \( \mu \). In fact, drift velocity = \( \mu E \) for holes = - \( \mu E \) for electrons.

Example: \( \mu_n = 1000 \text{ cm}^2/\text{v-sec} \) (or 10Km2/KV-sec) \( \mu_p = 500 \text{ cm}^2/\text{v-sec} \).

But at high electric fields, the average speed of carriers is NOT proportional to the field; that is the mobility concept fails. In fact, velocity saturates at 107 cm/sec = 100 km/sec for both electrons and holes.

This saturation is observable directly in the “resistance” of a silicon resistor at high fields (10KV/cm = 1V/\( \mu \)m).

THE “CHARGE CONTROL DEVICE”
OR
HOW TO MAKE A SMART SWITCH

Concept: Apply positive voltage to gate with respect to semiconductor. This will induce +Q on gate, -Q on surface of semiconductor. Resistance between D and S will drop.

Thus, we can control current from D to S.

CHARGE-CONTROL EXPERIMENT – “THE FIELD EFFECT”

Above some ‘threshold’ voltage \( V_T \), the number of electrons per square cm under the gate is proportional to \( V_G - V_T \), i.e., the charge \( Q_n \) is proportional to \( V_G - V_T \).

\[ Q_n = \varepsilon A (V_G - V_T) \]

These charge carriers can carry current from D to S, so we can make low resistance (RDS) by making \( V_G - V_T \) very large.

I-V CHARACTERISTICS IN THE LOW VDS REGIME

Consider first gate current and drain current versus GATE voltage.

The gate is insulated, so there can never be any gate current.
I-V CHARACTERISTICS IN THE LOW V_DS REGIME

Consider \( I_{DS} \), the current from D to S:

Below "threshold" no charge, no conduction. \((V_{GS} < V_T)\)
Above threshold \((V_{GS} > V_T)\), \( Q \) appears so drain to source conduction is possible

Very low resistance \((R_{DS})\) for increasing gate voltage \((V_{GS} \gg V_T)\)

We have a controlled switch!

I-V CHARACTERISTICS IN LOW V_DS REGIME (cont.)

MOS is just a (linear) controlled resistor in the low \( V_{GS} \) regime with the drain-to-source resistance depending on how much voltage is applied to the gate (compared to threshold).

Example of a device characteristic for low \( V_{GS} \):

\[
I_{DS} \propto V_{GS} - V_T
\]

CLEARLY A "CONTROLLED SWITCH"

Saturation Current NMOS Model

Current \( I_{OUT} \) only flows when \( V_{IN} \) is larger than the threshold value \( V_{TH} \) and the current is proportional to \( V_{OUT} \) up to \( V_{OUT-SAT-D} \) where it reaches the saturation current

\[
I_{OUT-SAT-D} = k_D (V_{IN} - V_{TH})^2 \quad \text{if} \quad V_{OUT} \geq V_{OUT-SAT-D}
\]

Note that we have added an extra parameter to distinguish between threshold \( V_{TH} \) and saturation \( V_{OUT-SAT-D} \).

Use these values in the homework.

Example:

\( k_D = 25 \mu A/V^2 \)
\( V_{TH} = 1V \)
\( V_{OUT-SAT-D} = 1V \)

\[
I_{OUT-SAT-D} = 25 \mu A (V_{IN} - 1)^2 \quad \text{if} \quad V_{OUT} \geq 1V
\]

State 3 \( V_{IN} = 3V \)

Linear \( (V_{OUT}) \)
Saturation \( (V_{OUT}) \)

And of course already know what happens to the I-V characteristics of short-channel MOS devices at higher values of \( V_{GS} \). We know that the curves "bend over" because of velocity saturation.