Calbot Contest Monday 5/12

Jason Gatt and Kevin Ha “Best in Show” in Tutbot/Calbot Contest F00

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Lecture Review

Review of Basic Circuit Concepts
Sheila Ross

Circuit Analysis
Transients
Logic
Timing Diagrams
Dependent Sources and Op-Amps
Load Line and \( V_{OUT} \) vs \( V_{IN} \)

Diodes
MOS Operation

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Example with both special cases

\[
\begin{align*}
I_1 & = \frac{V_a - V_d}{R_1} - \frac{V_a}{R_2 + R_3} \quad R_4 \frac{V_d + V_a}{R_4} = 0
\end{align*}
\]

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How to Combine Gate to Produce a Desired Logic Function?
(More basic Logical Synthesis)

Example:

\[
\begin{array}{ccc}
\text{A} & \text{B} & \text{C} & \text{F} \\
0 & 0 & 0 & 0 \\
0 & 0 & 1 & 1 \\
0 & 1 & 0 & 0 \\
0 & 1 & 1 & 0 \\
1 & 0 & 0 & 0 \\
1 & 0 & 1 & 1 \\
1 & 1 & 0 & 1 \\
1 & 1 & 1 & 0 \\
\end{array}
\]

\[ F = \overline{A} \overline{B} \overline{C} + AB\overline{C} \]

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Logical Synthesis
Guided by DeMorgan’s Theorem

DeMorgan’s Theorem:

\[ A + B + C = \overline{A \overline{B} \overline{C}} \quad \text{or} \quad \overline{A + B + C} = \overline{A} \overline{B} \overline{C} \]

Example of Using DeMorgan's Theorem:

\[ F = A \bullet B + C \bullet D \bullet E = \overline{A} \overline{B} \overline{C} \overline{D} \overline{E} \]

Thus any sum of products expression can be immediately synthesized from NAND gates alone.

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Logical Synthesis of XOR

F = A \cdot \overline{B} + \overline{A} \cdot B

We Need a Timing Diagram!

Delay 1
Delay 2
Delay 3

A
B

X = \overline{A} \cdot B

Y = A \cdot B

F

Timing Diagram for Delays in Logic

Logic level F = 1 F = 0

A
B
\overline{A}
\overline{B}
X
Y
F
time

EXAMPLE CIRCUIT: INCREASED OUTPUT RESISTANCE

Add resistor R_e

The input has been assumed to be shorted

Analysis: apply I_{TEST} and evaluate V_{TEST}

Unknowns: I_{TEST}, V_{TEST}, R_e

Need 3 equations to find the ratio of I_{TEST} / V_{TEST}

Intuitive Explanation: GmV_{IN} burps current which has to also go through R_0. This raises V_{TEST} and the output impedance V_{TEST}/I_{TEST}

TIMING DIAGRAMS

Show transitions of variables vs time

Note \tau becomes valid one gate delay after B switches

Note that \overline{B \cdot C} becomes valid two gate delays after B & C switch, because the invert function takes one delay and the NAND function a second.

No change at t = 3\tau

CASCADE OP-AMP CIRCUITS

How do you get started on finding V_{OUT}?

Hint: Identify Stages

Hint: I_{Q} does not affect V_{OUT}

See the further examples of op-amp circuits in the reader
**Composite Current Plot for the 42PD Circuit with 200kΩ Load to Ground**

- **State 1**: $V_{OUT}(V) = 5$
- **State 3**: $I_{OUT}(\mu A) = 20$
- **State 5**: $V_{THEVENIN}(200k\Omega) = 3.3 V$

**Voltage Transfer Function for the 42PD Logic Circuit w/wo Load**

- **State 1**: $V_{IN}(V)$ = 0
- **State 3**: $I_{OUT}(\mu A)$ = 0
- **State 5**: $V_{OUT}(V)$ = 5

**DIODE I-V CHARACTERISTICS AND MODELS**

- Simple "Perfect Rectifier" Model
  - If we can ignore the small forward-bias voltage drop of a diode, a simple effective model is the "perfect rectifier," whose I-V characteristic is given below:

**Feedback Can Provide Memory**

- Carriers per unit volume
- Carrier mobility
- Resistance
- Resistivity

**COOL THINGS A DIODE CAN DO**

- "Rectified" version of input waveform

**Physics of Current Flow, Resistance, Resistivity**

- $E = V/L$
- $I = V/R$
- $R = \rho L/A = (1/q \mu N) L/W t = (L/W) \rho q N t$
- Carriers per unit volume
- Carriers per unit area
- Resistance of a "square" of the film
Relation of Current to Physical Parameters

\[ I_D = \mu_C \left( \frac{W}{L} \right)_n (V_{GS} - V_T)^n \cdot V_{OUT-SAT}^{-e} \]

- Mobility of carriers
- Oxide thickness
- Voltage of scattering velocity limit
- Excess Gate drive
- Geometrical Layout

\[ \mu_n = \frac{500 \text{ (cm}^2 / \text{Vs})}{25 \text{ (cm)}} \]
\[ \mu_p = \frac{150 \text{ (cm}^2 / \text{Vs})}{25 \text{ (cm)}} \]

\[ C_{ox} = \frac{8.85 \times 10^{-14} \text{ F/cm}}{6 \times 10^{-3} \text{ cm}} = 5.75 \times 10^{-7} \text{ F/cm} \]

\[ V_{OUT-SAT-n} = E_{Gm} \cdot L = 10^4 \text{ (V/cm)} \cdot 0.25 \times 10^{-4} \text{ cm} = 0.25V \]