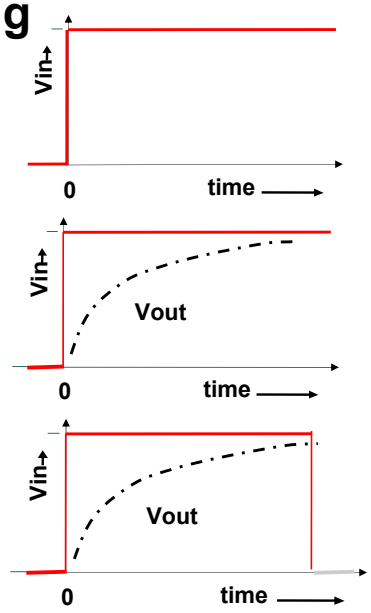
Lecture 13

Today we will

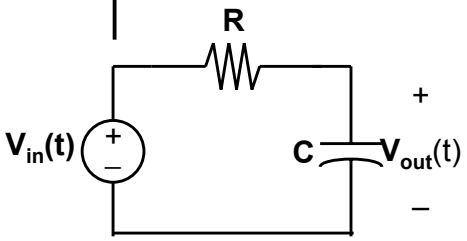
- Examine how the logic gate model (RC circuit) reacts to a sequence of input changes
- Relate these results to clocking speed
- Define propagation delay
- Introduce digital logic gates
- Examine how signals propagate through logic circuits

Sequential Switching

- What if we step up the input to a logic circuit,
- wait for the output to respond,
- then bring the input back down to perform the next computation?



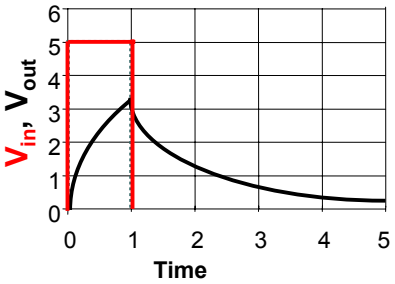
Pulse Distortion



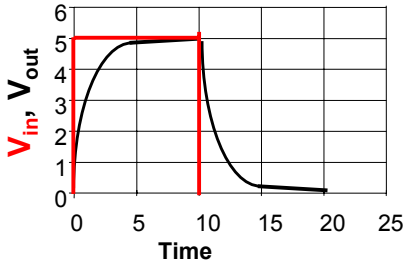
We need to wait for the output to reach a recognizable logic level, before changing the input again.

This affects clock speed.

Pulse width = *RC*

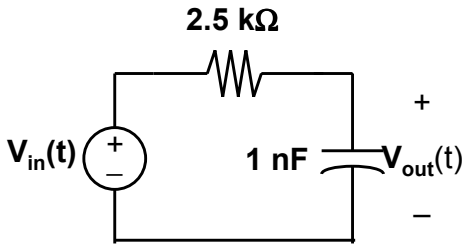


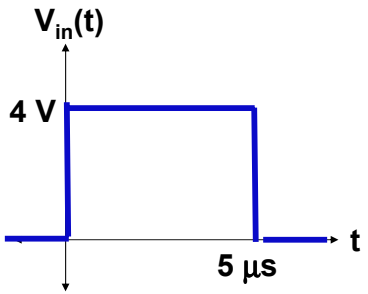
Pulse width = 10*RC*



Example

- Suppose that the capacitor is discharged at t=0.
- With $V_{in}(t)$ as shown, find $V_{out}(t)$.





Example

- First, $V_{out}(t)$ will approach 4 V exponentially.
- We write the equation for this part using:
  - Initial condition $V_{out}(0) = 0$ V
  - Final value $V_{out,f} = 4$ V
  - Time constant RC = (2.5 kΩ)(1 nF) = 2.5 μs

$$V_{out}(t) = V_{out,f} - (V_{out}(0) - V_{out,f})e^{-t/RC}$$

$$V_{out}(t) = 4 - 4e^{-t/2.5\mu s} \text{ V} \quad \text{for } 0 \le t \le 5\ \mu s$$

Example

- Then, at 5 μs, $V_{out}(t)$ will approach 0 V exponentially.
- We write the equation for this part using:
  - Initial condition $V_{out}(5\ \mu s) = ?$
    Use equation from previous step, since V_{out} is continuous.

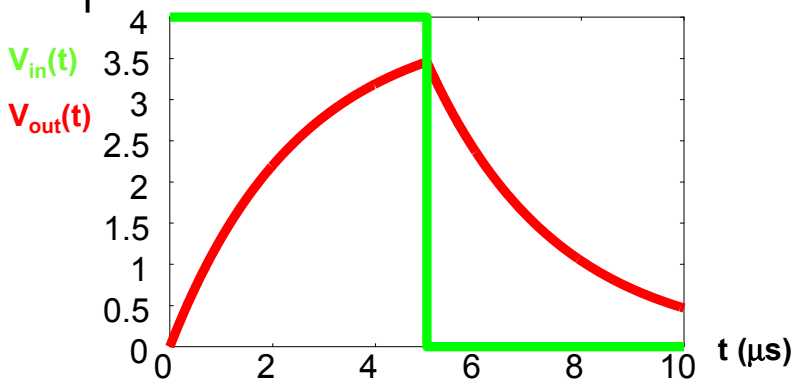
$$V_{out}(5\mu s) = 4 - 4e^{-5\mu s/2.5\mu s} = 3.44 \text{ V}$$

  - Final value $V_{out,f} = 0$ V
  - Time constant RC = (2.5 kΩ)(1 nF) = 2.5 μs

$$V_{out}(t) = V_{out,f} - (V_{out}(t_0) - V_{out,f})e^{-(t-t_0)/RC}$$

$$V_{out}(t) = 3.44e^{-(t-5\mu s)/2.5\mu s} \qquad \text{for } t > 5\ \mu s$$

Example



$$V_{out}(t) = \begin{cases} 4\text{-}4e^{-t/2.5\mu s} \text{ for } 0 \le t \le 5\ \mu s \\ 3.44e^{-(t-5\mu s)/2.5\mu s} \text{ for } t > 5\ \mu s \end{cases}$$

Design Issues

- How long between successive inputs?
  - Need output to reach recognizable logic level
  - Output must be at this level long enough to serve as input to next logic gate
- How many consecutive logic gates does signal go through before being “cleaned up” or saved in static memory cell?
  - Eventually the signal gets really bad
  - But adding hardware adds cost and delay

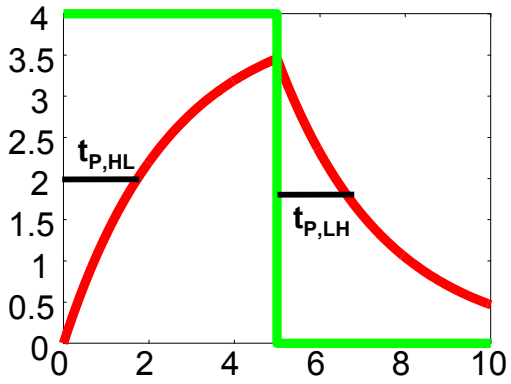
Propagation Delay

- Suppose an input goes from some initial voltage to some final voltage.
- In our examples, the input switch is immediate, but in practice it is not.
- Propagation delay is officially defined as:

  (time when output is halfway to final value) **minus**

  (time when input is halfway to final value)

Illustration



$t_{P,HL} = t_{P,LH} = 1.725\ \mu s$

Using our equation for $V_{out}(t)$, we can find:

$t_{P,HL}$
(time when $V_{out}(t) = 2$ V, as it goes from 0 V to 4 V) – 0 s

$t_{P,LH}$
(time when $V_{out}(t) = 1.72$ V, as it goes from 3.44 V to 0 V) – 5 μs

Propagation Delay

- It's not a coincidence that the propagation delays were the same.
- For a general RC circuit that has an input voltage switch at $t = t_0$,

  $V_{out}(t) = V_{out,f} - (V_{out}(t_0) - V_{out,f})e^{-(t-t_0)/RC}$
- The time when $V_{out}(t)$ is $\frac{1}{2}(V_{out,f} + V_{out}(t_0))$ is given by

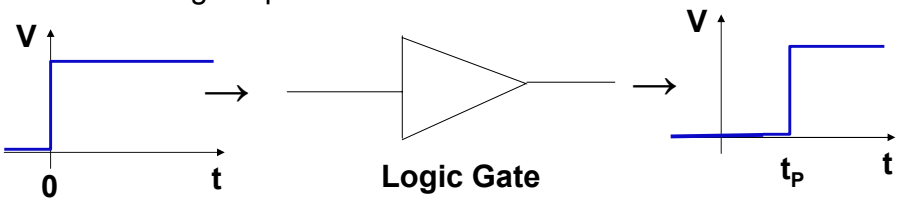
  $\frac{1}{2}(V_{out,f} + V_{out}(t_0)) = V_{out,f} - (V_{out}(t_0) - V_{out,f})e^{-(t-t_0)/RC}$
- Simplifying,

  $\frac{1}{2} = e^{-(t-t_0)/RC}$ $\quad t = (\ln 2)(RC) + t_0$
- The propagation delay, the difference between this time and t_0, is

  $t_P = (\ln 2)(RC)$ Depends only on time constant!

Graphing Propagation through Multiple Logic Gates

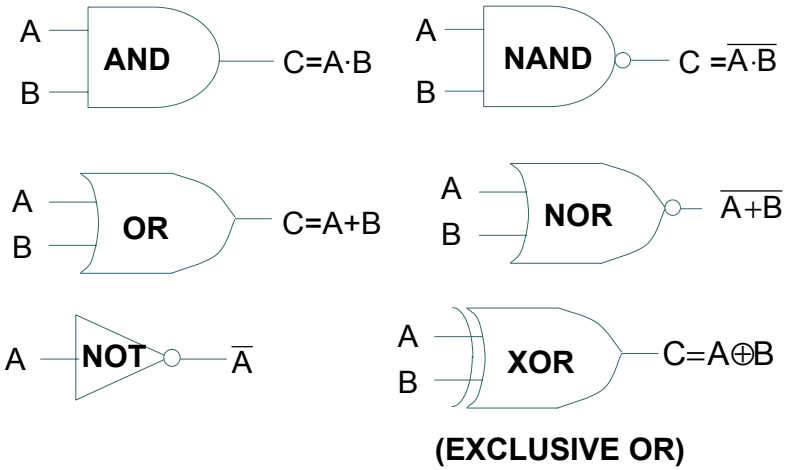
- We will want to examine how these RC-related delays affect a signal going through multiple logic gates.
- The math involved in putting an RC output (decaying exponential) into another RC circuit is not so easy.
- So, when analyzing a circuit with many logic gates, we will use the following simplification:



Logic Gates

- We have been using a simple RC circuit to model a logic gate.
- In each case, the final value of V_{out} was V_{in}.
- This will not always be true; sometimes, the output will go to logic 0 when the input is logic 1 and vice-versa.
- To determine what the final value of a logic gate output will be, we need to learn the types of logic gates.

Logic Gates



(EXCLUSIVE OR)

Logic Functions: Truth Tables

We specify what a logic circuit does by listing the output for each possible input. This listing is called a **truth table.**

A	$\overline{A}$
0	1
1	0

NOT

A	B	A·B	$\overline{A \cdot B}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

AND NAND

Logic Functions: Truth Tables

A	B	A+B	$\overline{A+B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

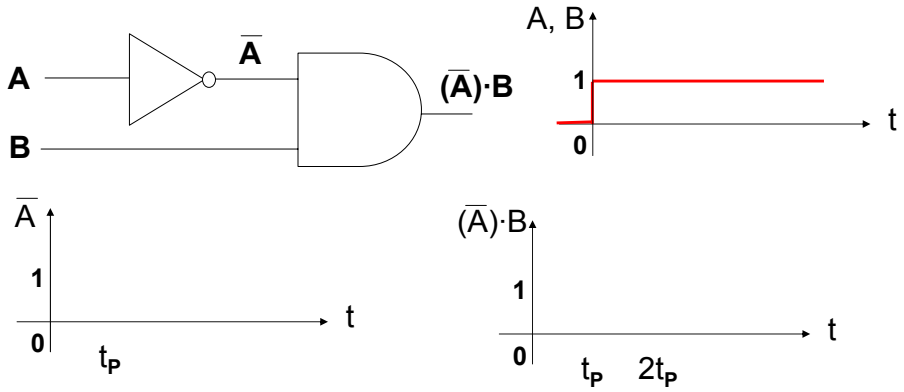
OR NOR

A	B	A ⊕B	$\overline{A \oplus B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

XOR XNOR

Timing Diagrams

- Now let's look at how signals propagate through logic gates, taking delay into consideration.
- Sketch the output for each logic gate in a more complicated circuit.

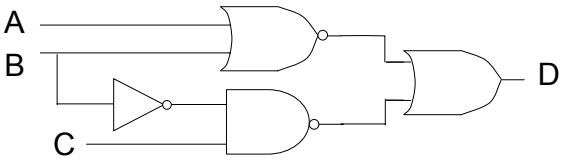


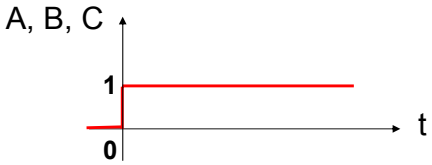
Strategy for Timing Diagrams

To find the output for a particular gate,

- Graph the inputs for that gate
- Graph the result of the logic gate using the input graphs
- Shift right by one t_P

Example





Example