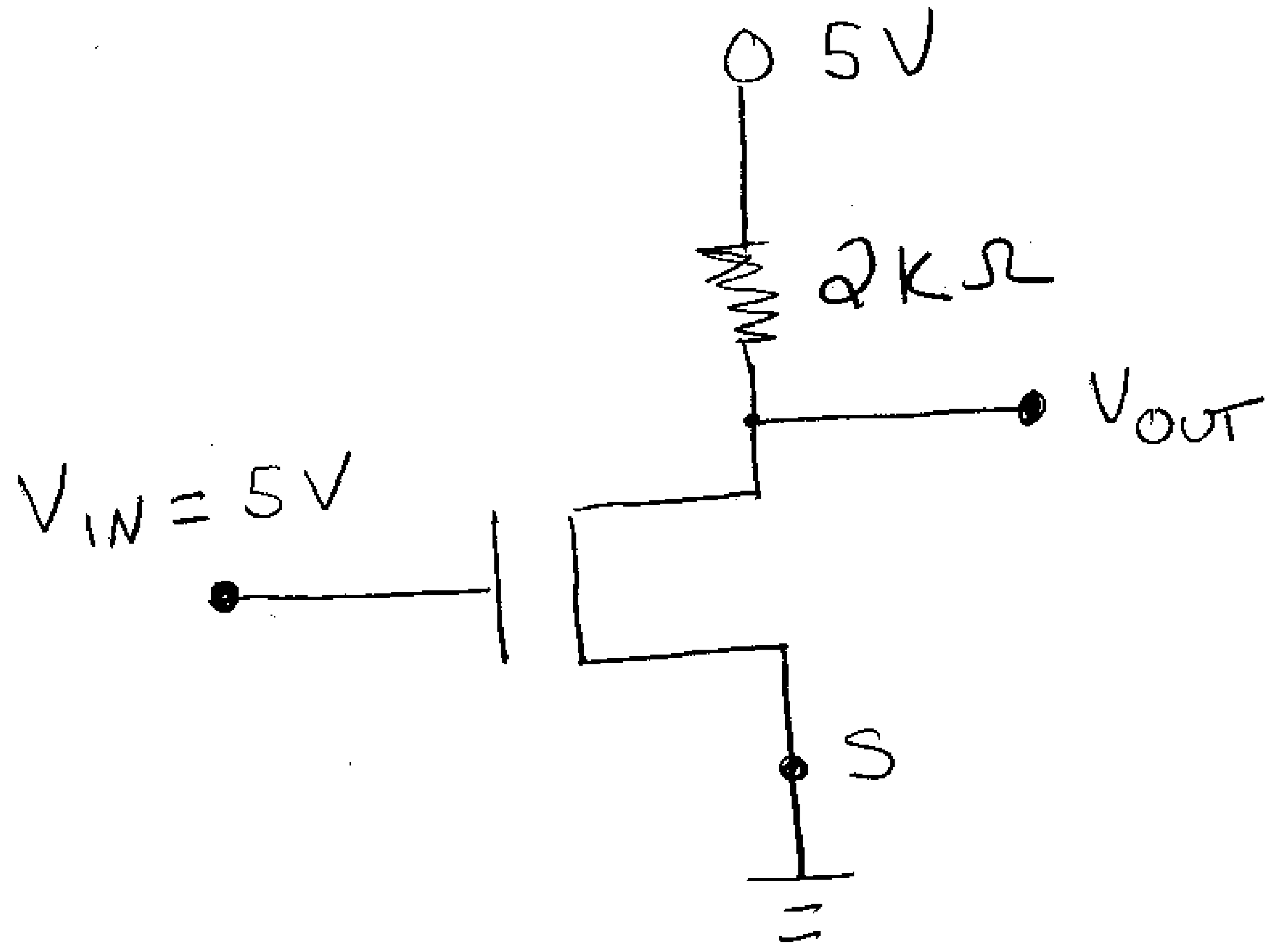
Lecture 18

NMOS and PMOS Circuits

Our general method for solution of transistor circuits:

1. Guess the mode for each transistor
   * If possible, try to see whether V_{GS} will exceed V_{TH}. You can often tell right away whether transistor is cutoff.
2. Write down the I-V relationship for each transistor, for the modes you guessed.
3. Write down KVL & KCL equations - enough so that you have a full set of equations.
4. Solve for V_{GS}, V_{DS}, and I_D.
5. Check to see if these values are possible for the mode that you guessed.
6. If yes, stop. If no, start over with new guesses.



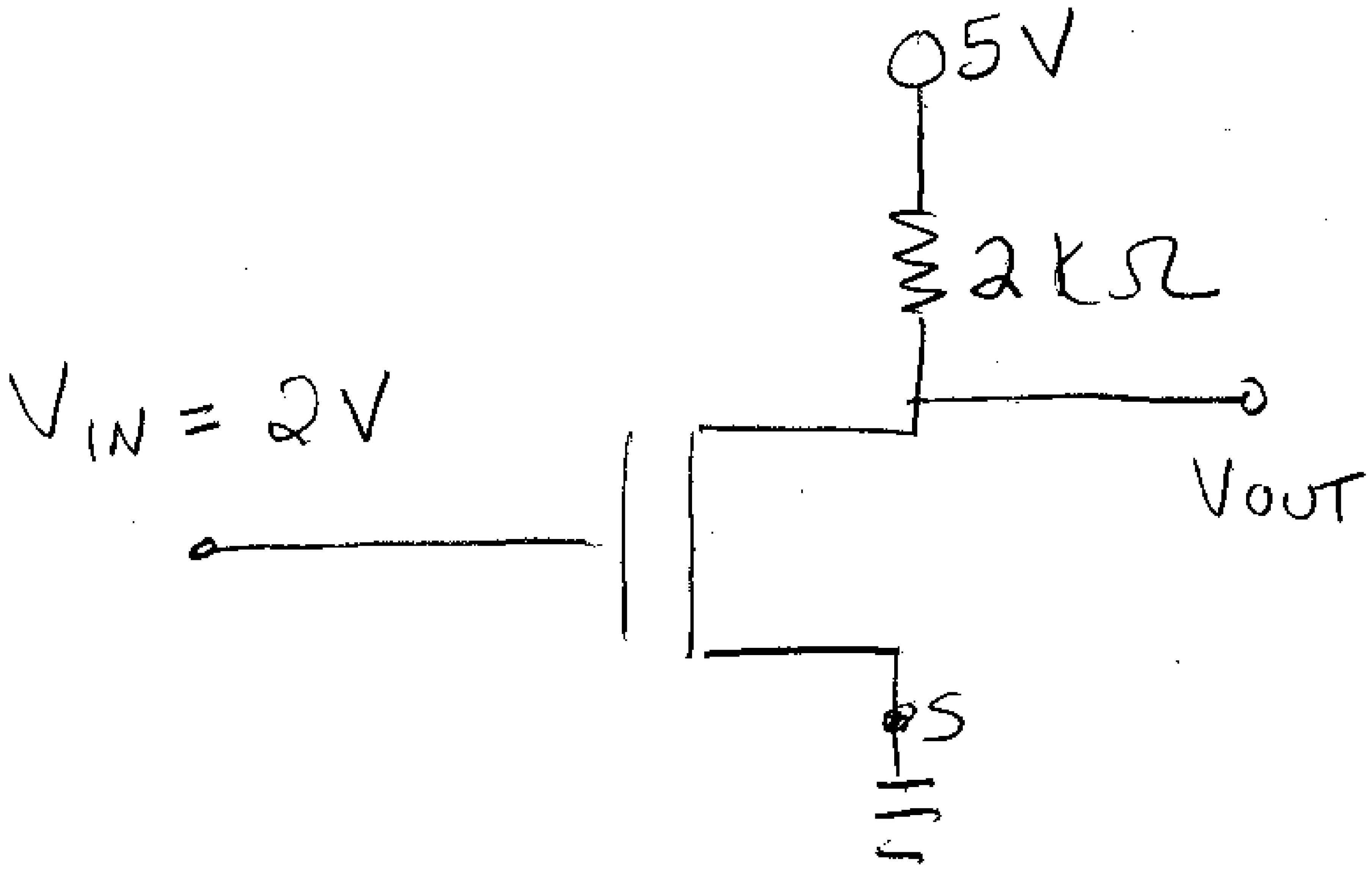
$V_{TH(n)} = 1V$

$\lambda_n = 0$

$\frac{W}{L}\mu_n C_{ox} = 1 mA/V^2$

Find V_{GS}, V_{DS}, I_D, and V_{out}.

(2)



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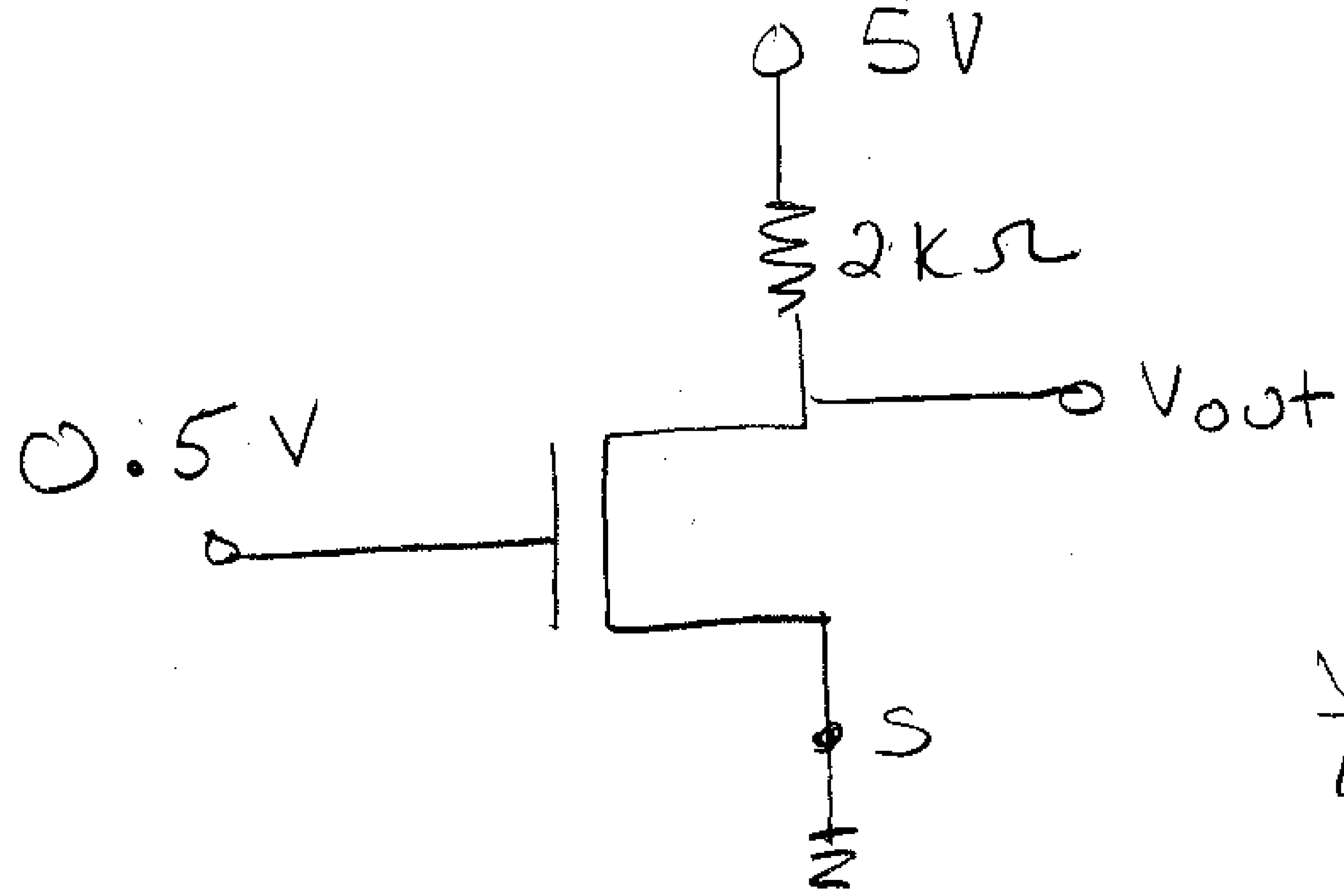
Find V_{GS}, V_{DS}, I_D & V_{OUT}.

(3)



$V_{TH(n)} = 1V$

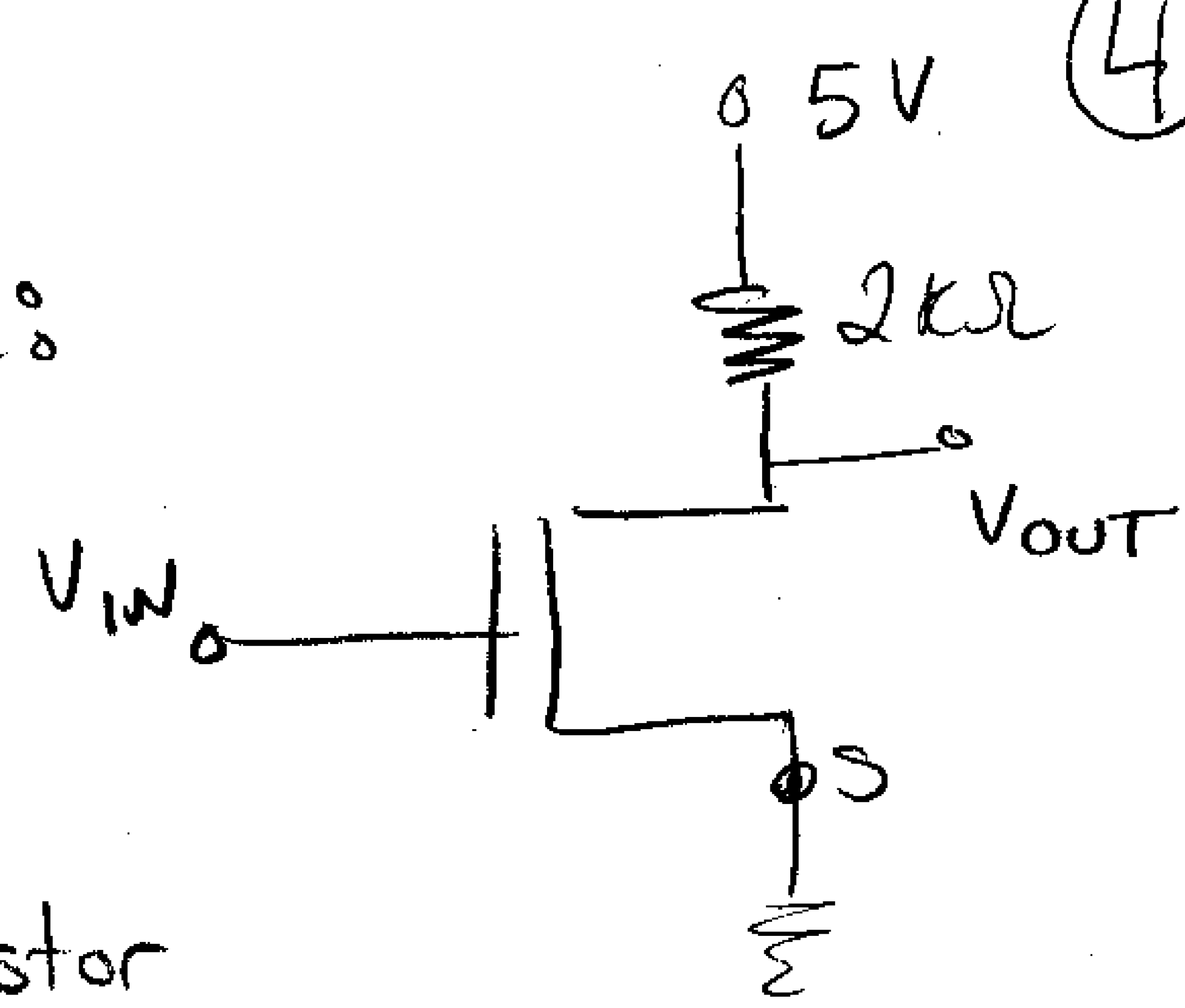
$\lambda_n = 0$

$\frac{W}{L}\mu_n C_{ox} = 1\ mA/V^2$

Find V_{GS}, V_{DS}, I_D & V_{OUT}.

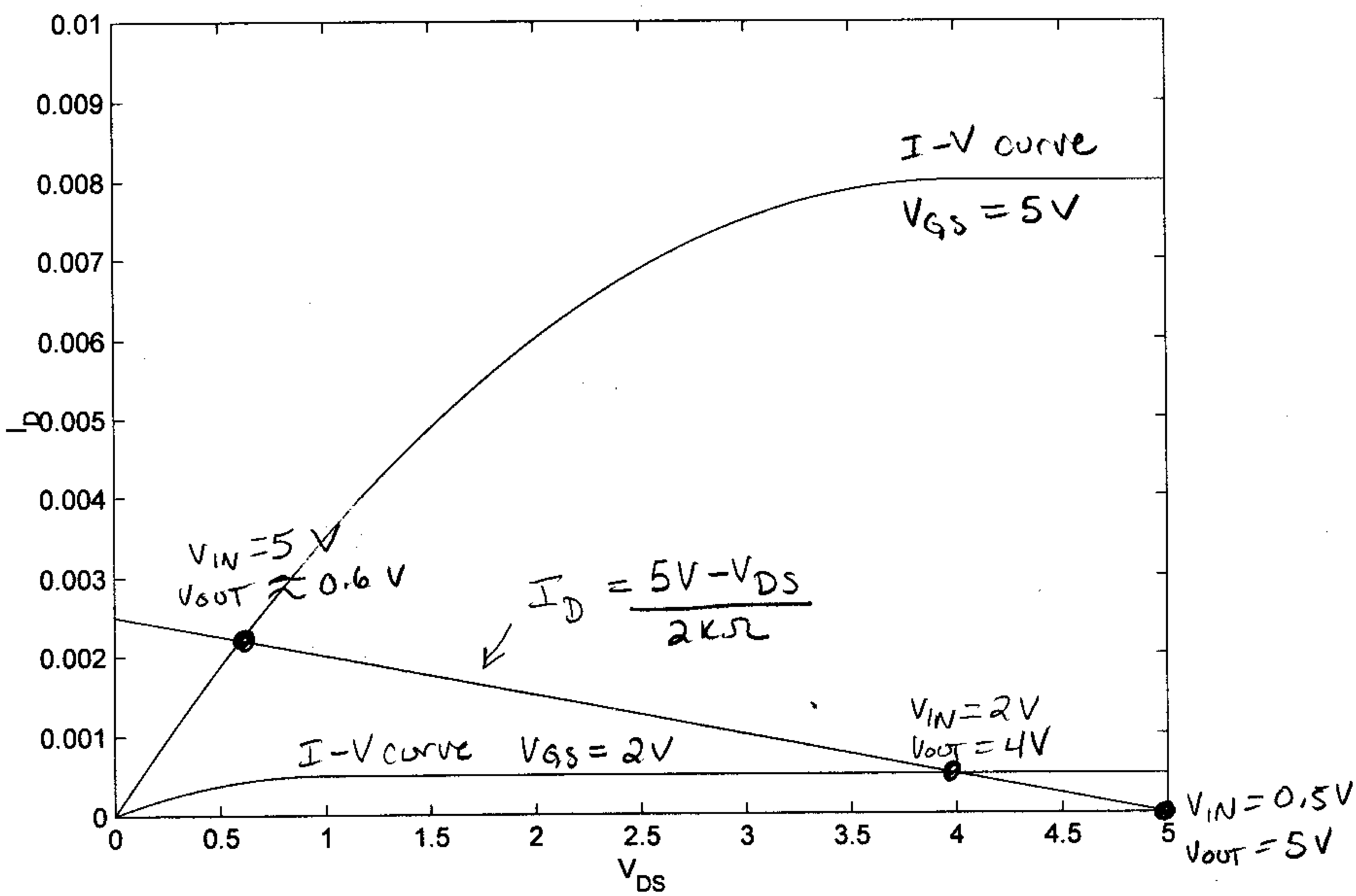
For this circuit, we always have the same KVL (Ohm's law) equation:

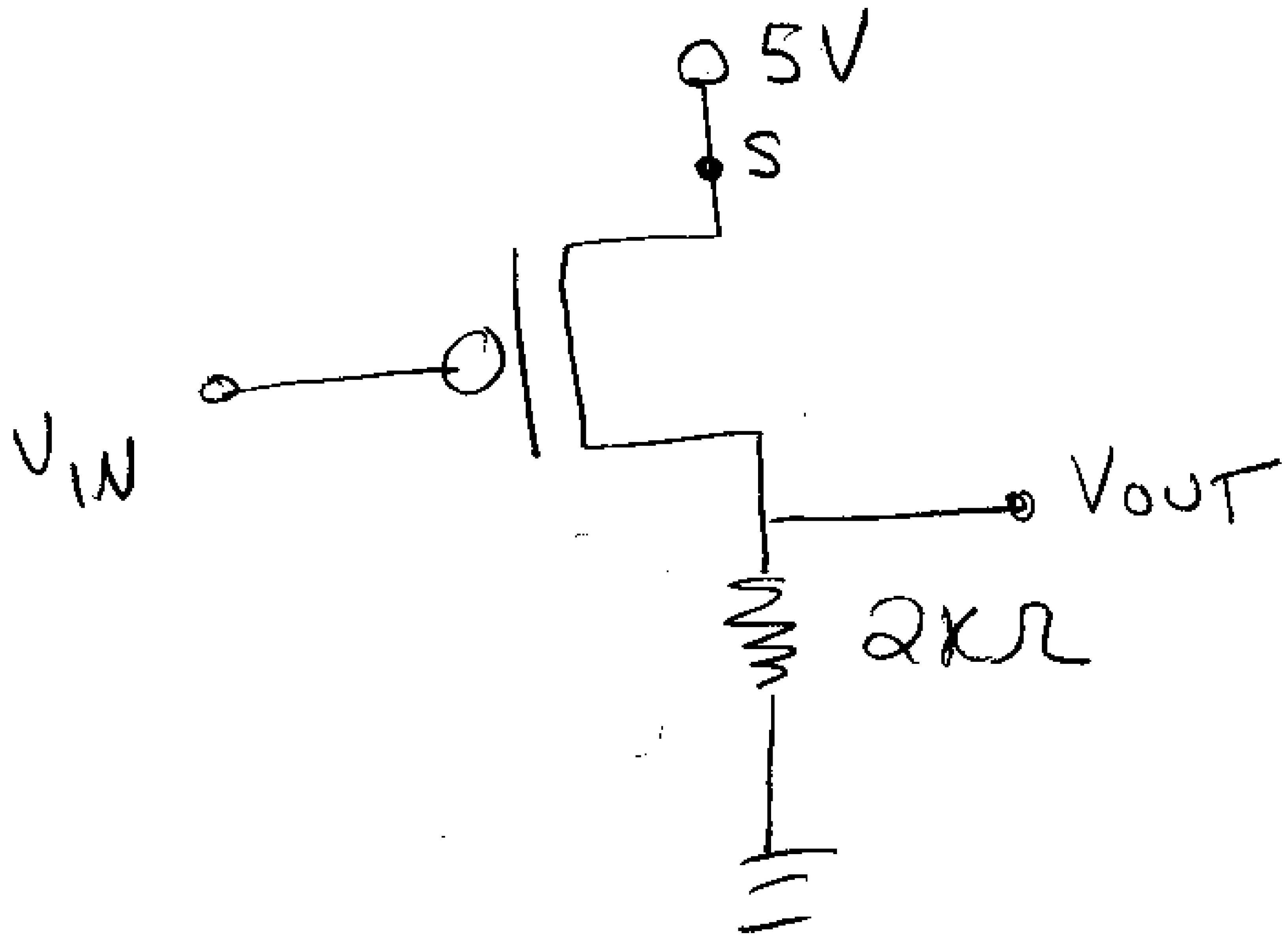
$$I_D = \frac{5V - V_{DS}}{2k\Omega}$$



The I-V curve for the transistor changes as V_{GS} changes.

When V_{GS} is big (V_{IN} is big), V_{DS} (V_{out}) is small. As V_{GS} (V_{IN}) decreases, the curve goes down, and the solution moves right – V_{DS} (V_{out}) increases. This is an <u>inverter</u>!





$V_{TH(p)} = -1V$

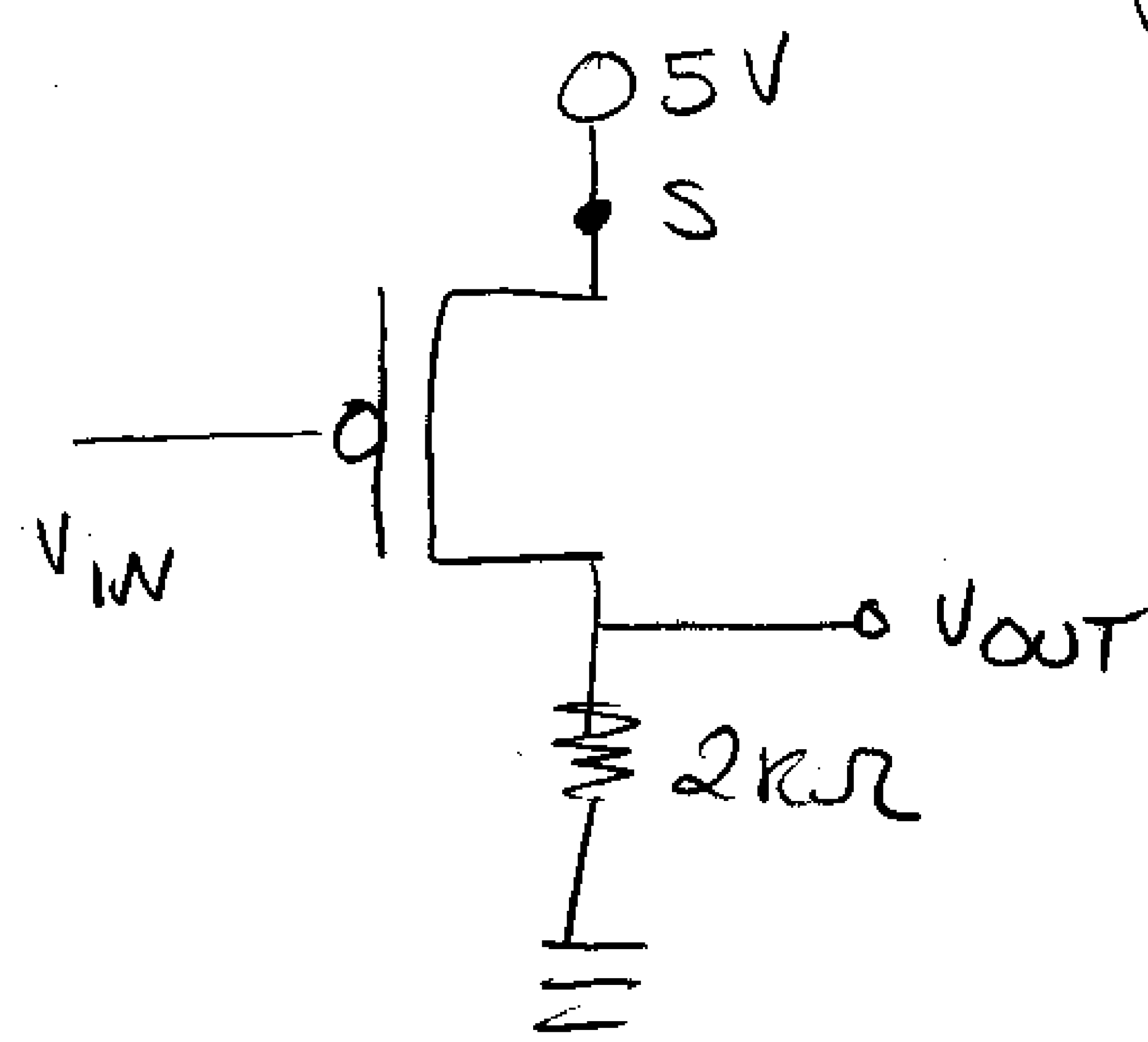
$\lambda_p = 0$

$\frac{W}{L} \mu_p C_{ox} = 1 \frac{mA}{V^2}$

This circuit is the complement of the NMOS inverter.

Find V_{OUT} for $V_{IN} = 4.5V$, $3V$, and $0V$.

We get the reverse picture as compared to the NMOS circuit.



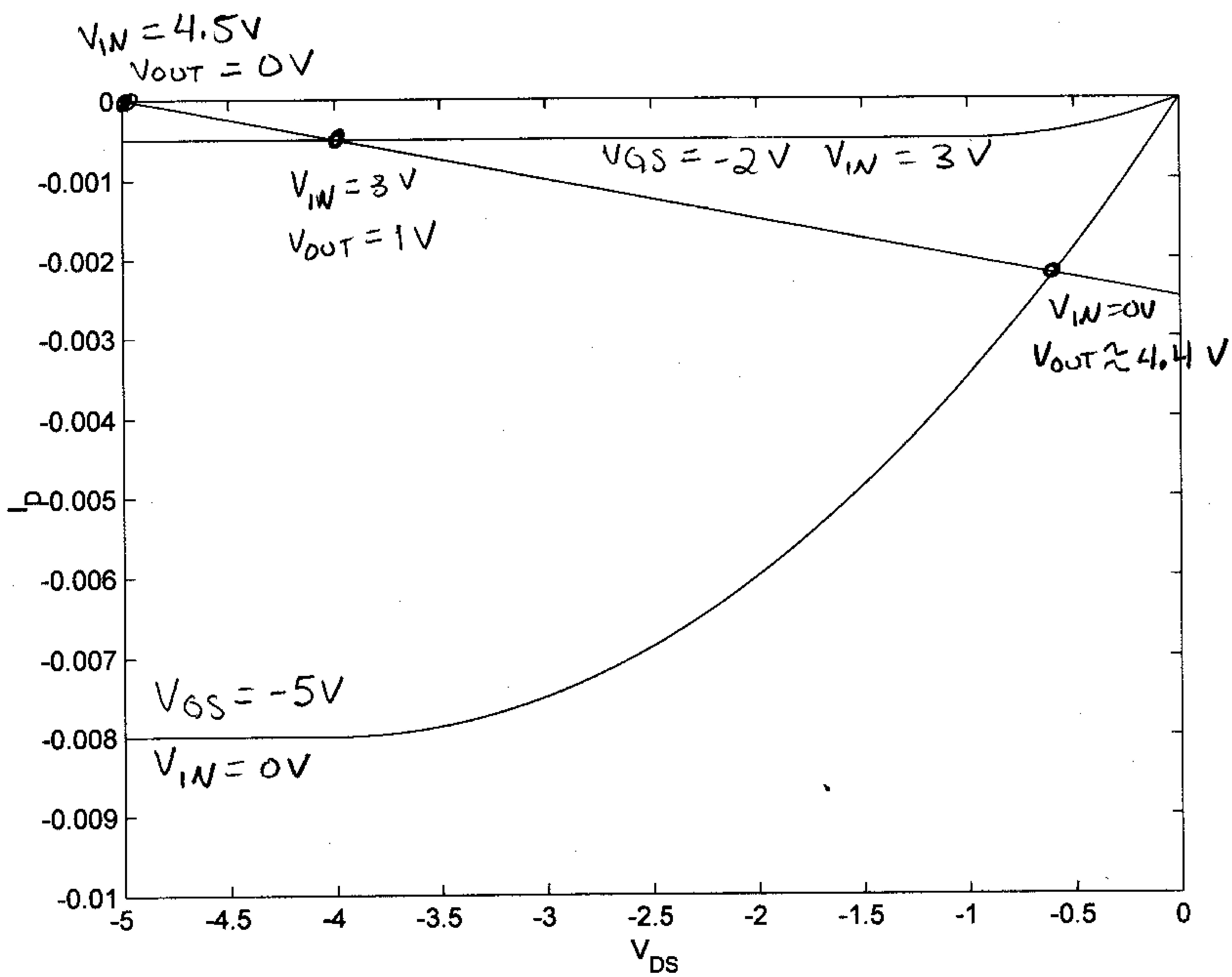
We have to be careful interpreting it, since

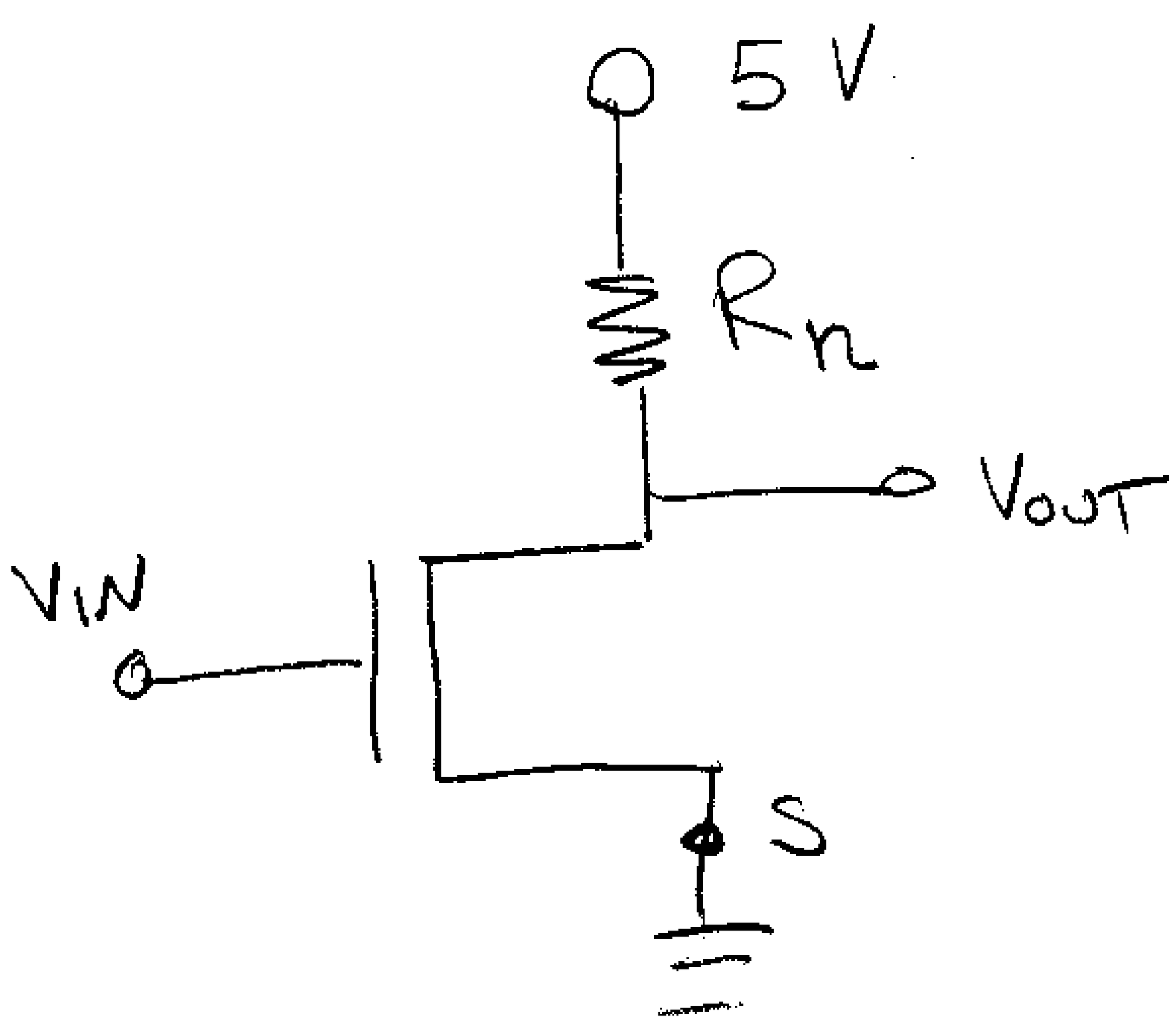
$V_{IN} = V_{GS} - 5V$

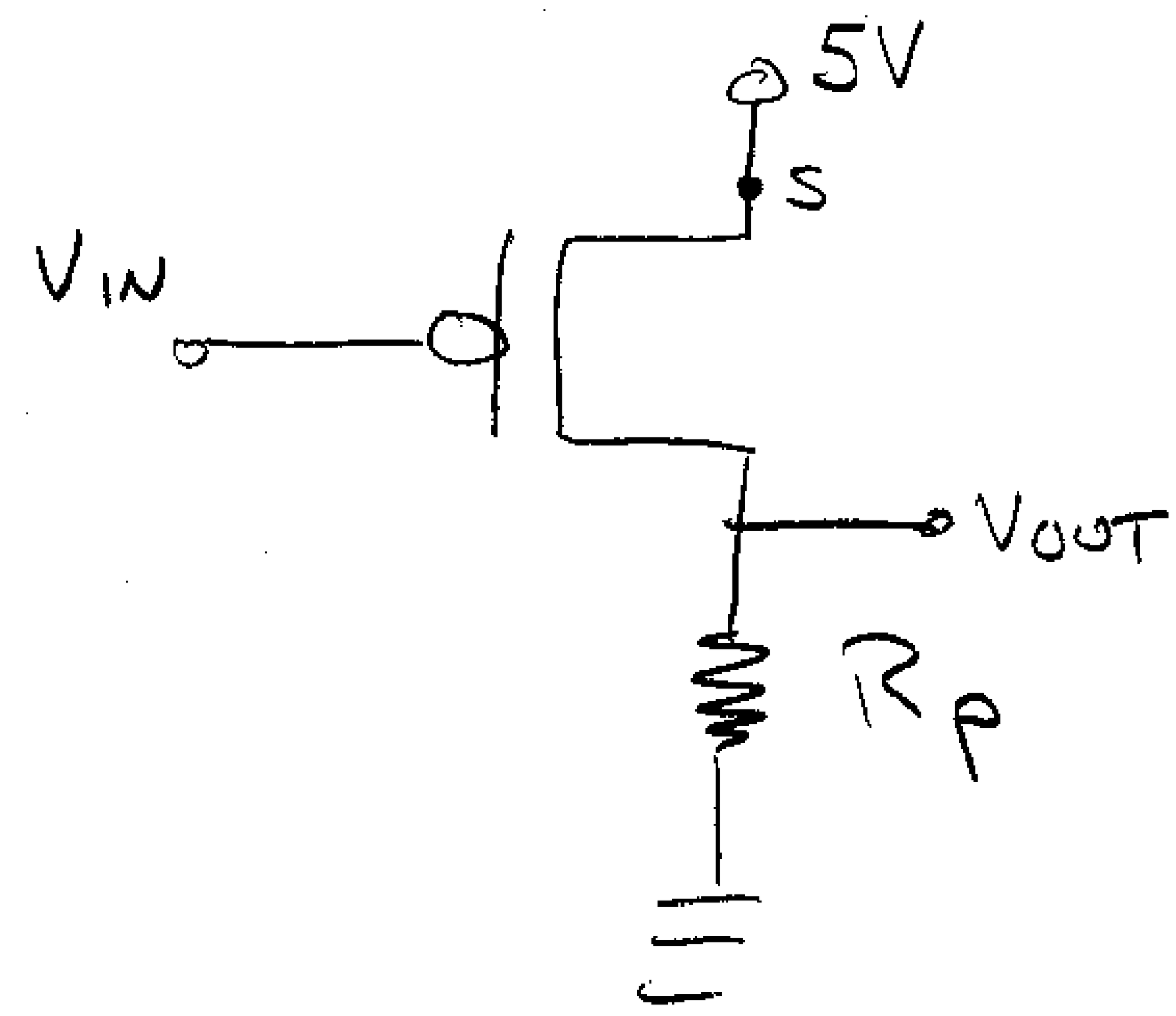
$V_{OUT} = V_{DS} + 5V$

When $V_{IN} \uparrow$, V_{GS} gets less negative. Curve moves up. Solution moves left. V_{DS} gets more negative. $V_{OUT} \downarrow$.

This is also an inverter!







R_n is called the "pull-up" resistor.

R_p is called the "pull-down" resistor.

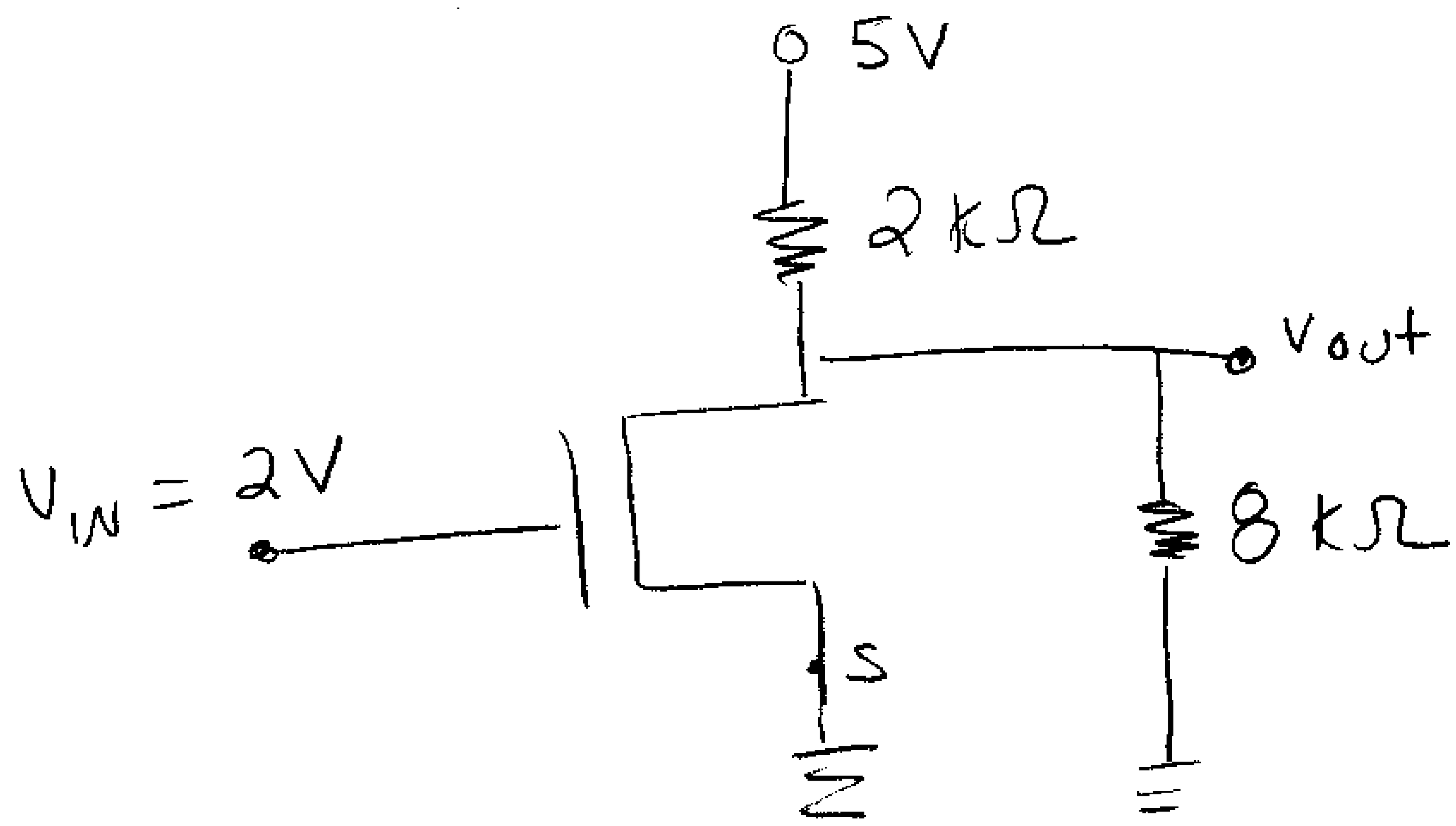
This terminology will make more sense when we study CMOS, but note that when the input to the NMOS circuit is low, NMOS is cutoff (acts like open circuit). The resistor "pulls" the output voltage up to 5V (since it has 0 V when $I_D = 0$).

When the input to the PMOS is high, the PMOS is cutoff, and R_p has 0V, "pulling" V_{OUT} to 0V.

But notice in the opposite circumstances, (V_{IN} high for NMOS or V_{IN} low for PMOS) there will be constant current flow through resistors. Burns power while not switching — CMOS will fix this!

Our inverters had open outputs.

If there is something (a "load") attached, the voltages & currents are different.



Find V_{GS}, V_{DS}, I_D & V_{OUT}.