Today we will:
- Look at why our NMOS and PMOS inverters might not be the best inverter designs
- Introduce the CMOS inverter
- Analyze how the CMOS inverter works

**NMOS Inverter**

When $V_{IN}$ changes to logic 0, the transistor gets cutoff. $I_D$ goes to 0.
Resistor voltage goes to zero. $V_{OUT}$ “pulled up” to 5 V.

When $V_{IN}$ is logic 1, $V_{OUT}$ is logic 0.
Constant nonzero current flows through transistor.
Power is used even though no new computation is being performed.
PMOS Inverter

When $V_{\text{IN}}$ is logic 0, $V_{\text{OUT}}$ is logic 1.

Constant nonzero current flows through transistor.

Power is used even though no new computation is being performed.

When $V_{\text{IN}}$ changes to logic 1, transistor gets cutoff. $I_D$ goes to 0. Resistor voltage goes to zero. $V_{\text{OUT}}$ “pulled down” to 0 V.

Analysis of CMOS Inverter

- We can follow the same procedure to solve for currents and voltages in the CMOS inverter as we did for the single NMOS and PMOS circuits.
- Remember, now we have two transistors so we write two I-V relationships and have twice the number of variables.
- We can roughly analyze the CMOS inverter graphically.

NMOS is “pull-down device”
PMOS is “pull-up device”
Each shuts off when not pulling
NMOS Inverter

Saturation mode

$V_{GS} = 3\, \text{V}$

$V_{GS} = 1\, \text{V}$

Linear $I_D$ vs $V_{DS}$ given by surrounding circuit

Linear KVL and KCL Equations

$V_{GS(n)} = V_{IN}$

$V_{GS(p)} = V_{IN} - V_{DD}$

$V_{GS(p)} = V_{DS(n)} - V_{DD}$

$I_{D(p)} = -I_{D(n)}$

$V_{DS(n)} = V_{OUT}$

$V_{DS(p)} = V_{OUT} - V_{DD}$

Use these equations to write both I-V equations in terms of $V_{DS(n)}$ and $I_{D(n)}$.
CMOS Analysis

As $V_{IN}$ goes up, $V_{GS(n)}$ gets bigger and $V_{GS(p)}$ gets less negative.

$V_{IN} =$  
$V_{GS(n)} =$ 0.9 V

As $V_{IN}$ goes up, $V_{GS(n)}$ gets bigger and $V_{GS(p)}$ gets less negative.

$V_{IN} =$  
$V_{GS(n)} =$ 1.5 V
CMOS Analysis

As \( V_{IN} \) goes up, \( V_{GS(n)} \) gets bigger and \( V_{GS(p)} \) gets less negative.

**NMOS I-V curve**

**PMOS I-V curve**

(written in terms of NMOS variables)

\[ V_{IN} = \]
\[ V_{GS(n)} = \]
\[ 2.0 \text{ V} \]

\[ V_{DS(n)} \]

\[ V_{DD} \]
CMOS Analysis

As $V_{IN}$ goes up, $V_{GS(n)}$ gets bigger and $V_{GS(p)}$ gets less negative.

NMOS I-V curve

PMOS I-V curve (written in terms of NMOS variables)

$V_{IN} = 3.0 \text{ V}$

$V_{GS(n)} = 3.0 \text{ V}$

$V_{DS(n)}$

$V_{DD}$

CMOS Analysis

As $V_{IN}$ goes up, $V_{GS(n)}$ gets bigger and $V_{GS(p)}$ gets less negative.

NMOS I-V curve

PMOS I-V curve (written in terms of NMOS variables)

$V_{IN} = 3.5 \text{ V}$

$V_{GS(n)} = 3.5 \text{ V}$

$V_{DS(n)}$

$V_{DD}$
CMOS Analysis

As $V_{IN}$ goes up, $V_{GS(n)}$ gets bigger and $V_{GS(p)}$ gets less negative.

PMOS I-V curve (written in terms of NMOS variables)

$V_{IN} = V_{GS(n)} = 4.1 \text{ V}$

CMOS Inverter $V_{OUT}$ vs. $V_{IN}$

curve very steep here; only in “C” for small interval of $V_{IN}$
**CMOS Inverter $I_D$**

**Important Points**

- No $I_D$ current flow in Regions A and E if **nothing** attached to output; current flows only during logic transition.
- If another inverter (or other CMOS logic) attached to output, transistor gate terminals of attached stage do not permit current; current still flows only during logic transition.