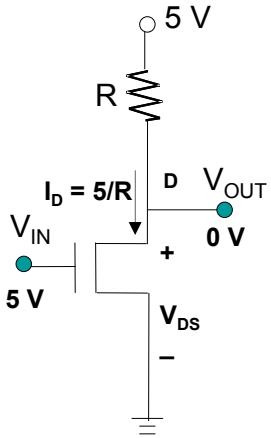
Lecture 20

Today we will

- Look at why our NMOS and PMOS inverters might not be the best inverter designs
- Introduce the CMOS inverter
- Analyze how the CMOS inverter works

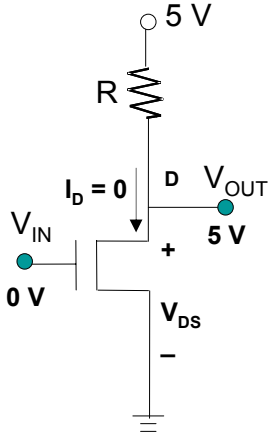
NMOS Inverter



When V_{IN} is logic 1, V_{OUT} is logic 0.

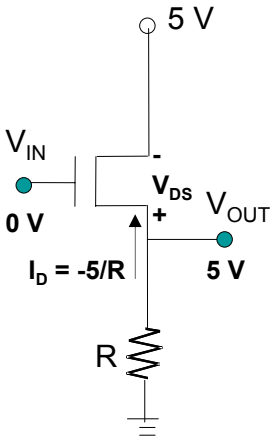
Constant nonzero current flows through transistor.

Power is used even though no new computation is being performed.



When V_{IN} changes to logic 0, transistor gets cutoff. I_D goes to 0. Resistor voltage goes to zero. V_{OUT} "pulled up" to 5 V.

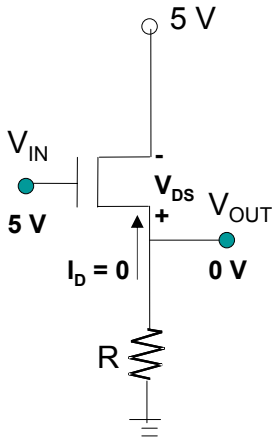
PMOS Inverter



When V_{IN} is logic 0, V_{OUT} is logic 1.

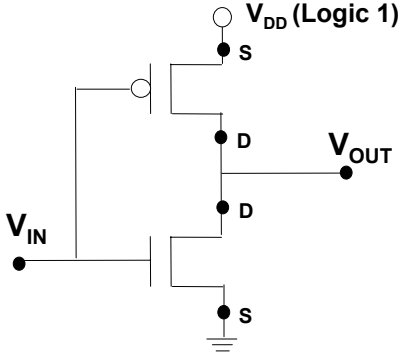
Constant nonzero current flows through transistor.

Power is used even though no new computation is being performed.



When V_{IN} changes to logic 1, transistor gets cutoff. I_D goes to 0. Resistor voltage goes to zero. V_{OUT} "pulled down" to 0 V.

Analysis of CMOS Inverter



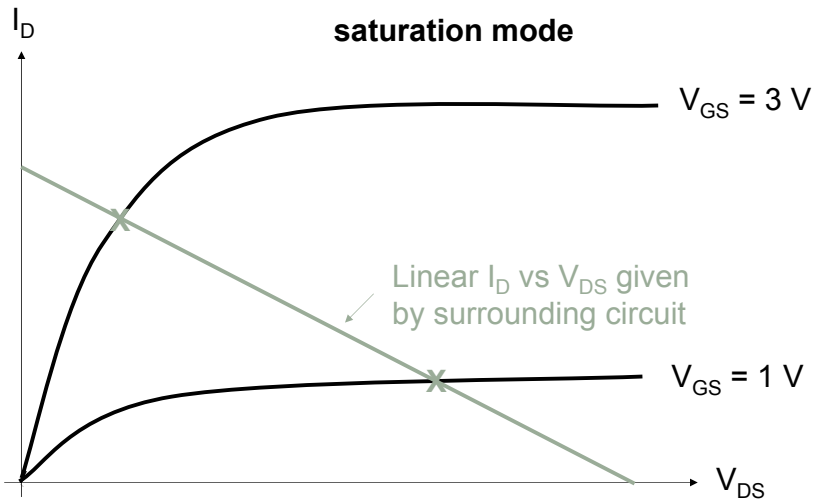
NMOS is "pull-down device"

PMOS is "pull-up device"

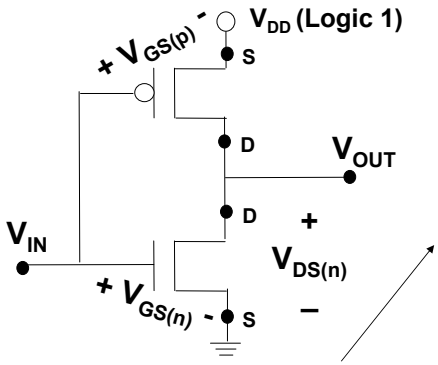
Each shuts off when not pulling

- We can follow the same procedure to solve for currents and voltages in the CMOS inverter as we did for the single NMOS and PMOS circuits.
- Remember, now we have **two transistors** so we write **two I-V relationships** and have **twice the number of variables**.
- We can roughly analyze the CMOS inverter graphically.

NMOS Inverter



Linear KVL and KCL Equations



$V_{GS(n)} = V_{IN}$

$V_{GS(p)} = V_{IN} – V_{DD}$

$V_{GS(p)} = V_{DS(n)} - V_{DD}$

$I_{D(p)} = -I_{D(n)}$

$V_{DS(n)} = V_{OUT}$

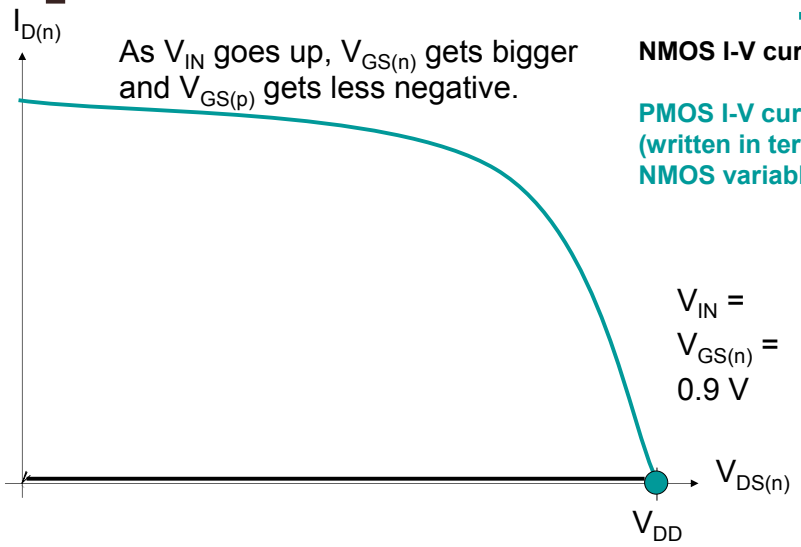
$V_{DS(p)} = V_{OUT} – V_{DD}$

$V_{DS(p)} = V_{DS(n)} - V_{DD}$

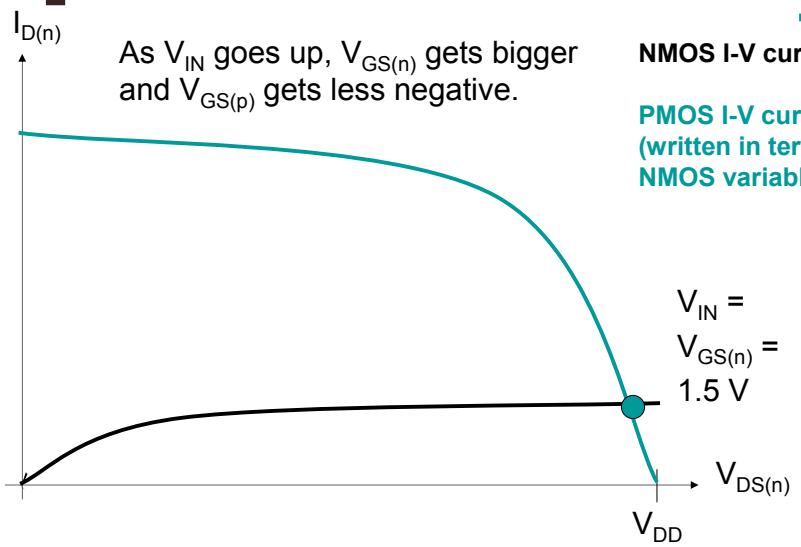
Use these equations

to write both I-V equations in terms of $V_{DS(n)}$ and $I_{D(n)}$

CMOS Analysis



CMOS Analysis

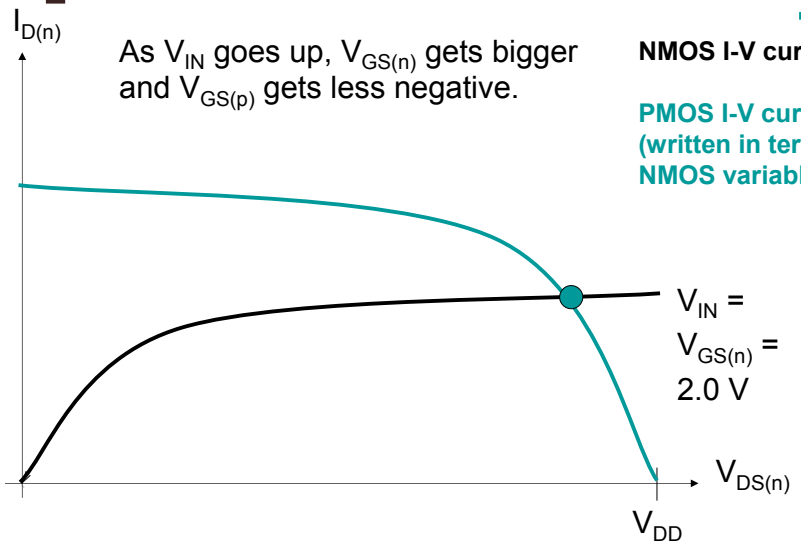


CMOS Analysis

As V_{IN} goes up, $V_{GS(n)}$ gets bigger and $V_{GS(p)}$ gets less negative.

NMOS I-V curve

PMOS I-V curve (written in terms of NMOS variables)

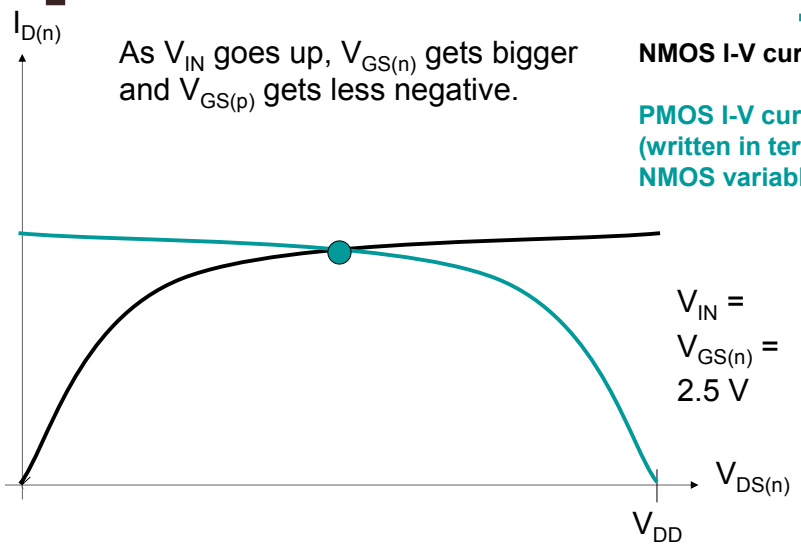


CMOS Analysis

As V_{IN} goes up, $V_{GS(n)}$ gets bigger and $V_{GS(p)}$ gets less negative.

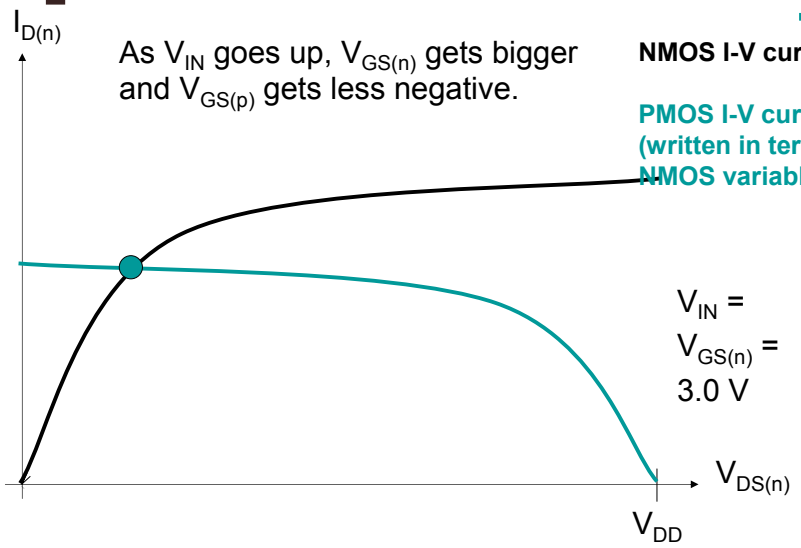
NMOS I-V curve

PMOS I-V curve (written in terms of NMOS variables)



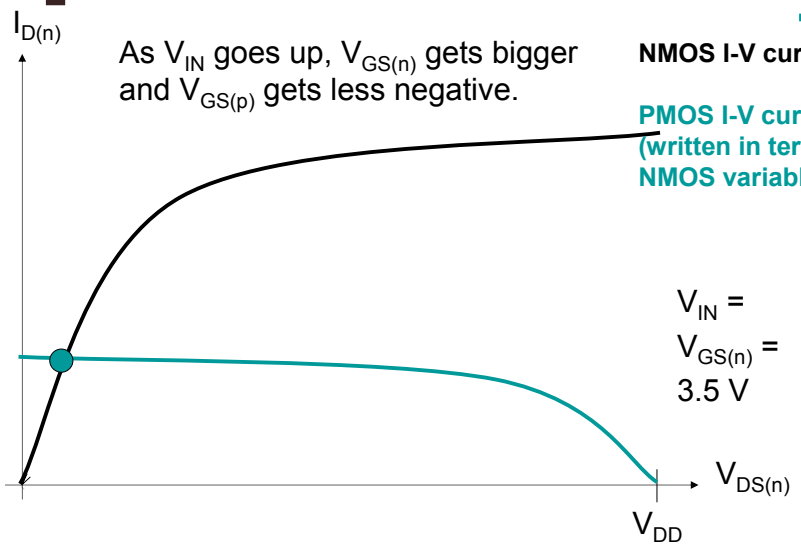
CMOS Analysis

As V_{IN} goes up, $V_{GS(n)}$ gets bigger and $V_{GS(p)}$ gets less negative.

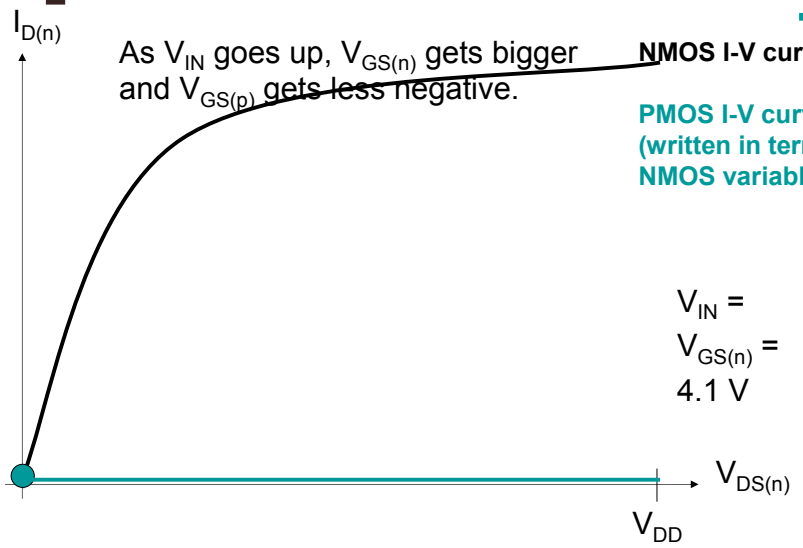


CMOS Analysis

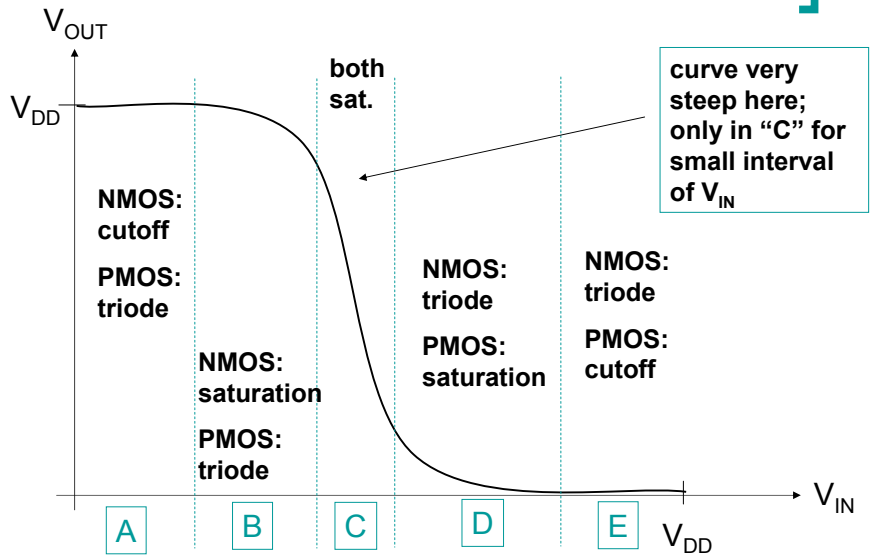
As V_{IN} goes up, $V_{GS(n)}$ gets bigger and $V_{GS(p)}$ gets less negative.



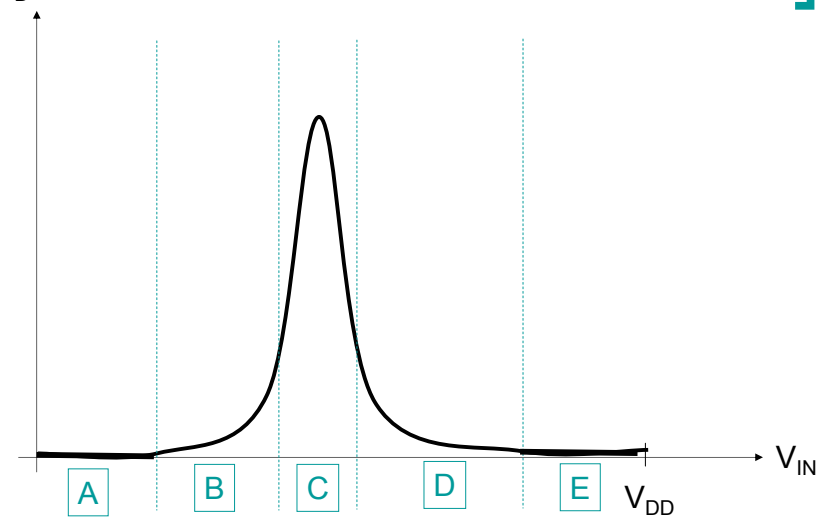
CMOS Analysis



CMOS Inverter V_{OUT} vs. V_{IN}



CMOS Inverter I_D



Important Points

- No I_D current flow in Regions A and E if **nothing** attached to output; current flows only during logic transition
- If another inverter (or other CMOS logic) attached to output, transistor gate terminals of attached stage do not permit current: current still flows only during logic transition