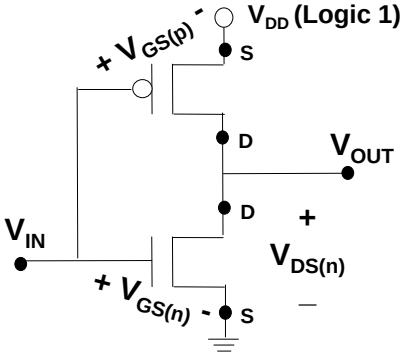
Lecture 21

Today we will

- Revisit the CMOS inverter, concentrating on logic 0 and logic 1 inputs
- Come up with an easy model for MOS transistors involved in CMOS digital computation
- Investigate the “complementary” nature of CMOS logic circuits
- Introduce CMOS NAND and NOR
- Determine the effective R and C for CMOS logic transitions

CMOS Inverter

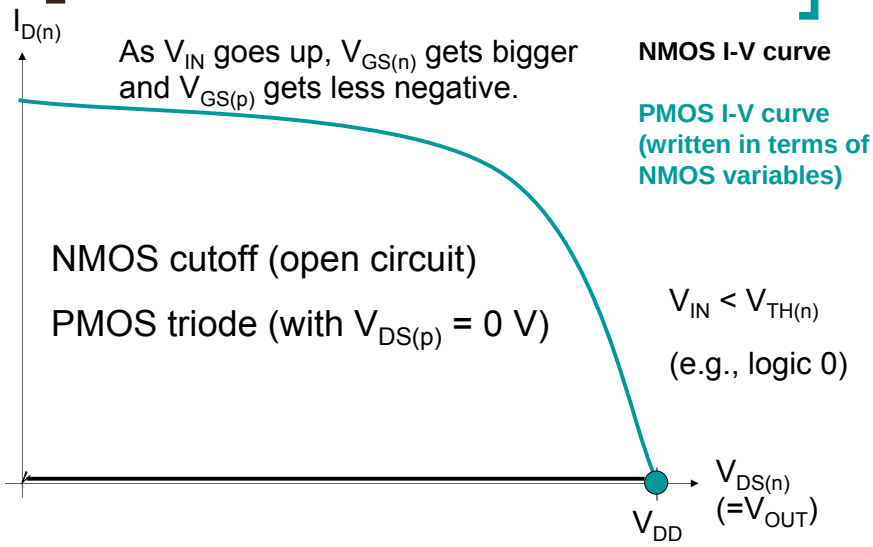


$V_{GS(n)} = V_{IN}$

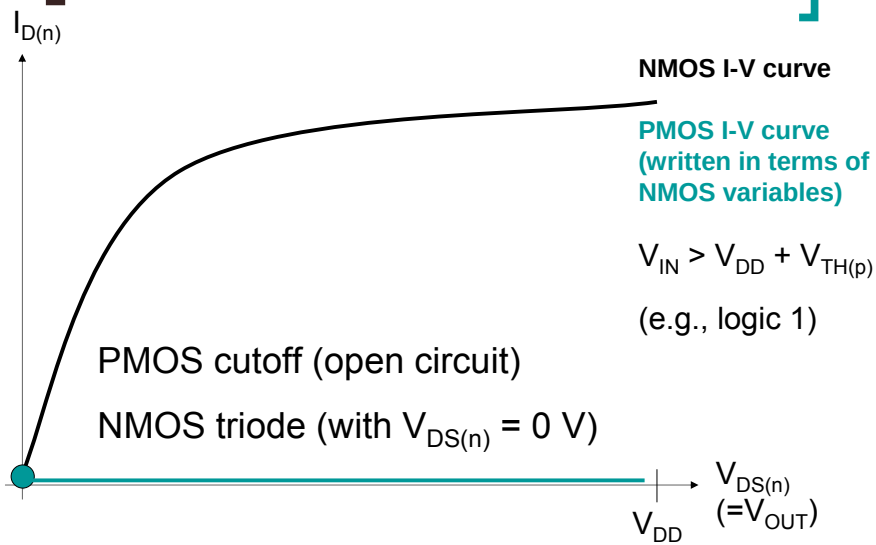
$V_{GS(p)} = V_{IN} – V_{DD}$

$V_{DS(n)} = V_{OUT}$

CMOS Analysis



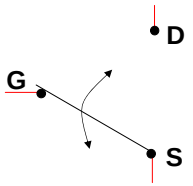
CMOS Analysis



Model for Digital Computation

- This leads us to a simpler model for transistors in CMOS circuits, **when V_{IN} is fully logic 0 or logic 1**.

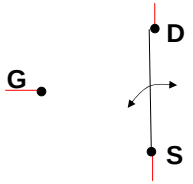
V_{GS} = 0 V



Transistor is cutoff.

Zero current flow.

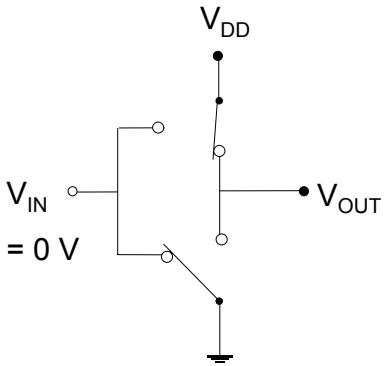
$V_{GS} = V_{DD}$ (for NMOS)
$V_{GS} = -V_{DD}$ (for PMOS)

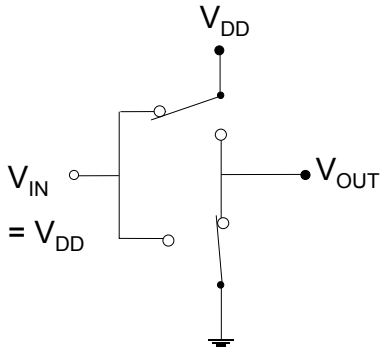


Transistor is not cutoff, but zero current flow of partner transistor causes V_{DS} = 0 V.

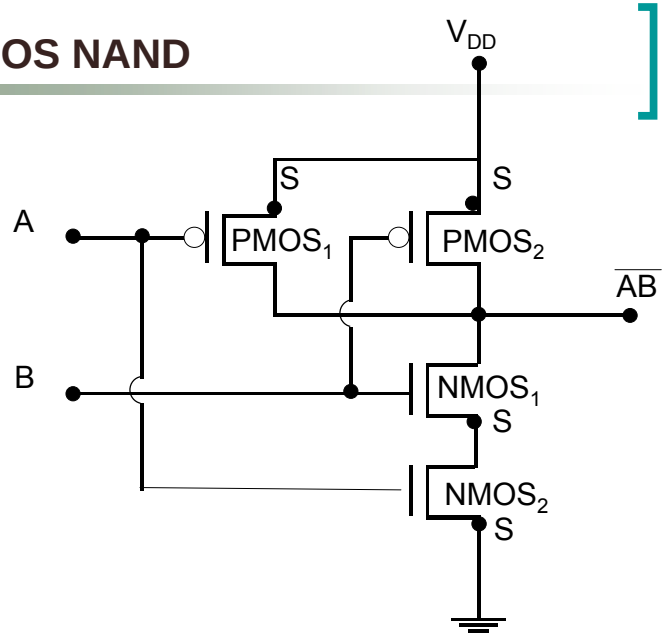
Practice

- Use this model to find V_{OUT} for the circuits below.



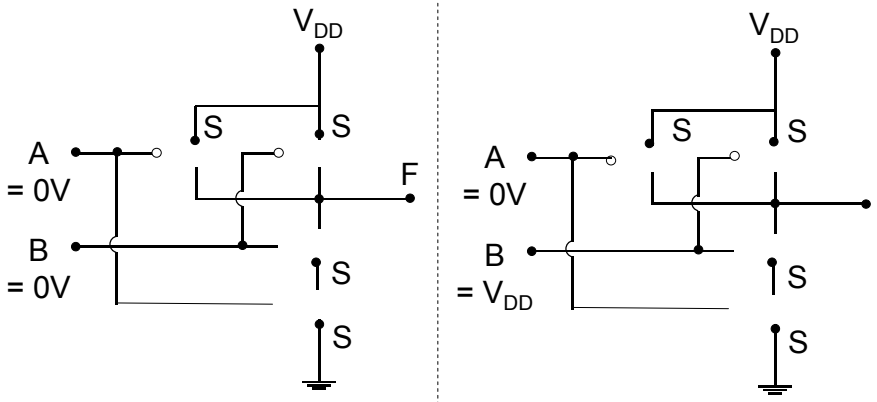


CMOS NAND



More Practice

Verify the logical operation of the CMOS NAND circuit:



More Practice

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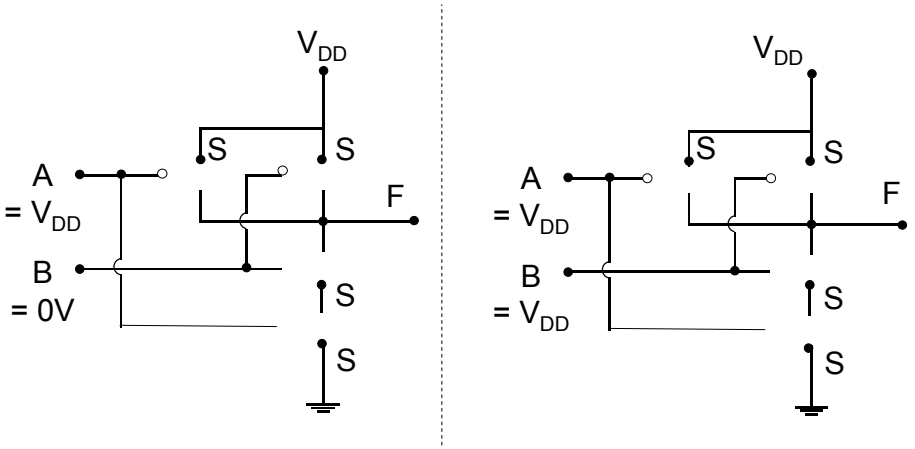
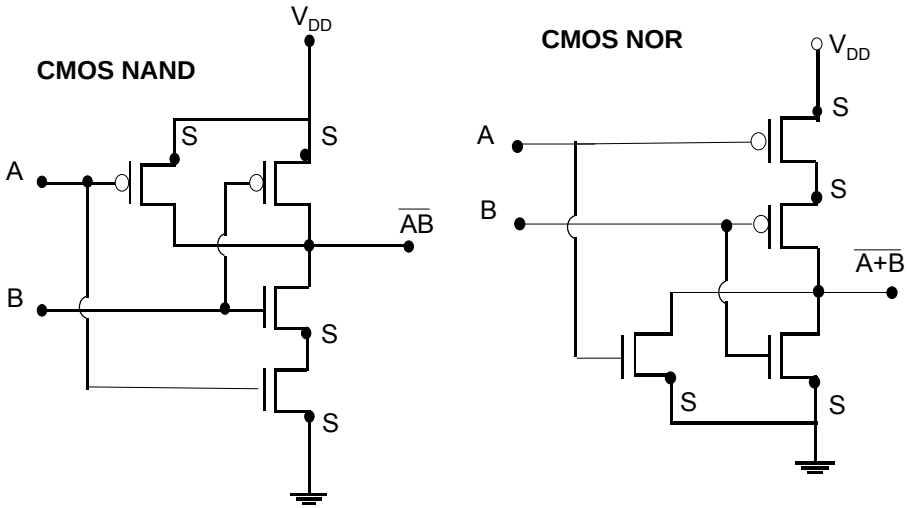


CMOS Networks

- Notice that V_{OUT} gets connected to either V_{DD} or ground by “active” (not cutoff) transistors.
- We say that these active transistors are “pulling up” or “pulling down” the output.
- NMOS transistors = **pull-down network**
- PMOS transistors = **pull-up network**
- These networks had better be **complementary** or V_{OUT} could be “floating”—or attached to both V_{DD} and ground at the same time.

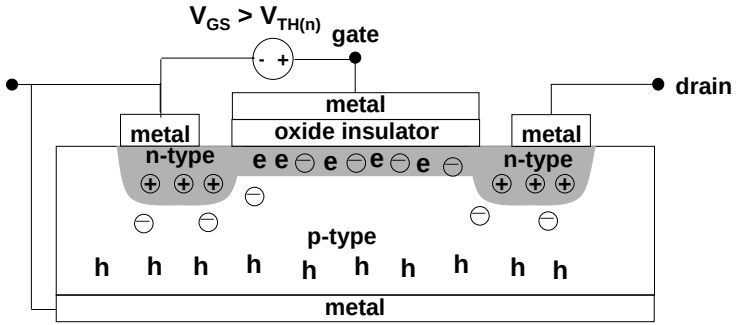
CMOS NAND vs. NOR



Complementary Networks

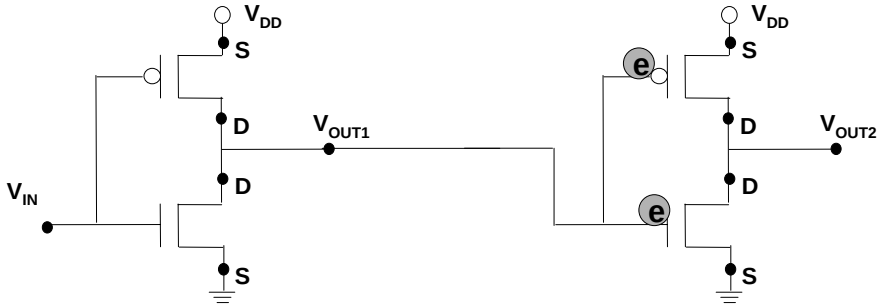
- If inputs A and B are connected to parallel NMOS, A and B must be connected to series PMOS.
- The reverse is also true.
- Determining the logic function from CMOS circuit is not hard:
  - Look at the NMOS half. It will tell you when the output is logic zero.
  - Parallel transistors: “like or”
  - Series transistors: “like and”

Resistance and Capacitance



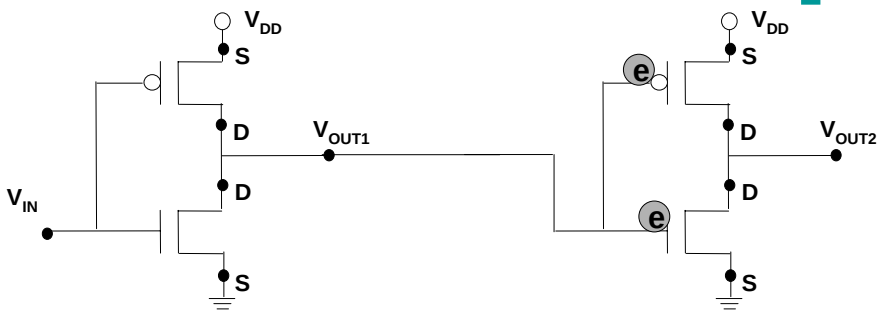
- The separation of charge by the oxide insulator creates a natural capacitance in the transistor from gate to source.
- The silicon through which I_D flows has a natural resistance.
- There are other sources of capacitance and resistance too.

Gate Delay—The Full Picture



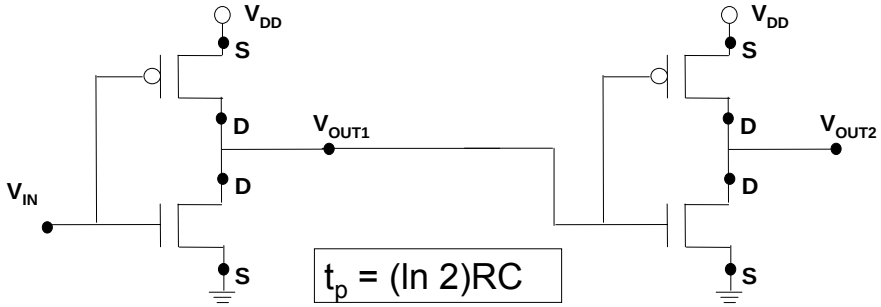
- Suppose V_{IN} abruptly changed from logic 0 to logic 1.
- V_{OUT1} may not change quickly, since is attached to the gates of the next inverter.
- These gates must collect/discharge electrons to change voltage.
- Each gate attached to the output contributes a capacitance.

Gate Delay—The Full Picture



- Where will these electrons come from/go to?
- No charges can pass through the cutoff transistor.
- Charges will go through the pull-down/pull-up transistors to ground. These transistors contribute resistance.

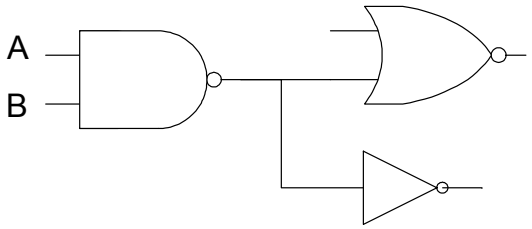
Computing Gate Delay



1. Determine the capacitance of each gate attached to the output. These combine in parallel. Higher **fan-out** = more capacitance.
2. Determine which transistors are pulling-up or pulling-down the output. Each contributes a resistance, and may need to be combined in series and/or parallel.
3. The C from 1) and R from 2) are the RC for the V_{OUT1} transition.

Example

- Suppose we have the following circuit:



Logic 0 = 0 V

Logic 1 = 1 V

NMOS resistance

R_n = 1 kΩ

PMOS resistance

R_p = 2 kΩ

Gate capacitance

C_G = 50 pF

- If A and B both transition from logic 1 to logic 0 at t = 0, find the voltage at the NAND output, $V_{OUT}(t)$, for $t \geq 0$.