\[ W_L \mu_n C_{ox} = \frac{W_L}{L \mu_p C_{ox}} = 1 \text{mA/V}^2 \]
\[ \lambda_n = \lambda_p = 0 \text{V}^{-1} \]
\[ V_{TH(n)} = 1 \text{V} \quad V_{TH(p)} = -1 \text{V} \]

\[ V_{DS(n)} + V_{DS(p)} + 5 \text{V} = 0 \quad J_{D(p)} + J_{D(n)} = 0 \]

Probably Region D: NMOS triode, PMOS saturation

\[ I_{D(p)} = -1 \text{mA/V}^2 \cdot \frac{1}{2} \cdot (2V - 1V)^2 = -\frac{1}{2} \text{mA} \]

\[ I_{D(n)} = 1 \text{mA/V}^2 \cdot (3V - 1V - \frac{V_{DS(n)}}{2}) V_{DS(n)} \]
\[ = -I_{D(p)} = \frac{1}{2} \text{mA} \]

\[ V_{DS(n)} = 3 \cdot 0.27 = 10.27 \text{V} \text{ ok for triode} \]
\[ V_{DS(p)} = V_{DS(n)} - 5 \text{V} = 0.27 \text{V} \text{ ok for saturation} \]

\[ V_{OUT} = 0.27 \text{V} \]
\[ V_{GS(n)} = 2V \quad V_{RH(p)} = -3V \]

\[ -V_{DS(n)} + V_{DS(p)} + 5V = 0 \quad I_{DM} + I_{D(p)} + I = 0 \]

\[ V_{DS(n)} = 5 \Omega I + 2V \] (in forward bias)

Guess NMOS in saturation, PMOS in triode

\[ I_{DP} = -1mA/\sqrt{2} (-3V + -1V - \frac{V_{DS(p)}}{2})V_{DS(p)} \]

\[ I_{D(n)} = \frac{1mA}{\sqrt{2}} (2V - 1V)^2 \cdot \frac{1}{2} = 1/2 mA \]

\[ = -I_{DP} - \frac{I}{2} \]

\[ = 1mA/\sqrt{2}(-2V - \frac{V_{DS(p)}}{2})V_{DS(p)} - \frac{V_{DS(n)} - 2}{5\Omega} \]

\[ = 1mA/\sqrt{2}(-2V - \frac{V_{DS(p)}}{2})V_{DS(p)} - \frac{V_{DS(p)} + 3}{5\Omega} \cdot \frac{-2V}{\sqrt{2}} \]

\[ V_{DS(p)} = \frac{3 - 3.82}{-0.58} \approx -6.3 \quad \text{For triode, need } V_{DS(p)} > V_{GS(p)} - V_{TH(p)} \]

\[ V_{DS(p)} = -0.58V \quad V_{DS(n)} = 4.42V \quad \text{ok for saturation} \]

\[ I = 0.484 mA \quad \text{ok for forward bias} \]

\[ V_{OUT} = 4.42V \]
Does this circuit perform a logic function?
If so, what function? (Give the Boolean expression).

No — if \( A = 0 \) and \( C = 1 \), then \( F \) is simultaneously connected to both \( V_{DD} \) and ground.
Does this circuit perform a logic function?
If so, what function? (Write the Boolean expression).

\[ F = \overline{A} \text{ when } A = 1 \text{ and } (B = 1 \text{ or } C = 1) \]

\[ \overline{F} = A(B + C) \Rightarrow F = \overline{A(B + C)} \]

Another way to write it:

\[ F = 1 \text{ when } A = 0 \text{ or } (B = 0 \text{ and } C = 0) \]

\[ F = \overline{A} + \overline{B} \overline{C} \text{ same as above (by DeMorgan)} \]
Suppose that for all \( t < 0 \), we had \( A = 1 \) and \( B = 0 \).

At \( t = 0 \), \( B \) goes (instantaneously) from 0 to 1.
Find \( V_{\text{out}}(t) \) and \( t_p \) for the first NAND gate.

\( V_{\text{out}} \) connected to 4 CMOS inputs.
Each input is 2-transistor gates. \( C_g = 4 \times 2 \times 20 \mu F = 160 \mu F \)

\[
R = R_n + R_p = 2 \times 10^3 \Omega
\]

\[
\tau_p = 1.2 \times 2 \times 10^3 \times 160 \mu F = 222 \text{ ns}
\]

Before: \( A = 1, B = 0 \) \( \Rightarrow V_{\text{in}} = 5 \text{ V} \)
After: \( A = 1, B = 1 \) \( \Rightarrow V_{\text{out}} = 0 \text{ V} \)

\[
V_{\text{out}}(t) = 0 + (5 - 0) e^{-t/320\text{ns}} = 5e^{-t/320\text{ns}} \text{ V}
\]