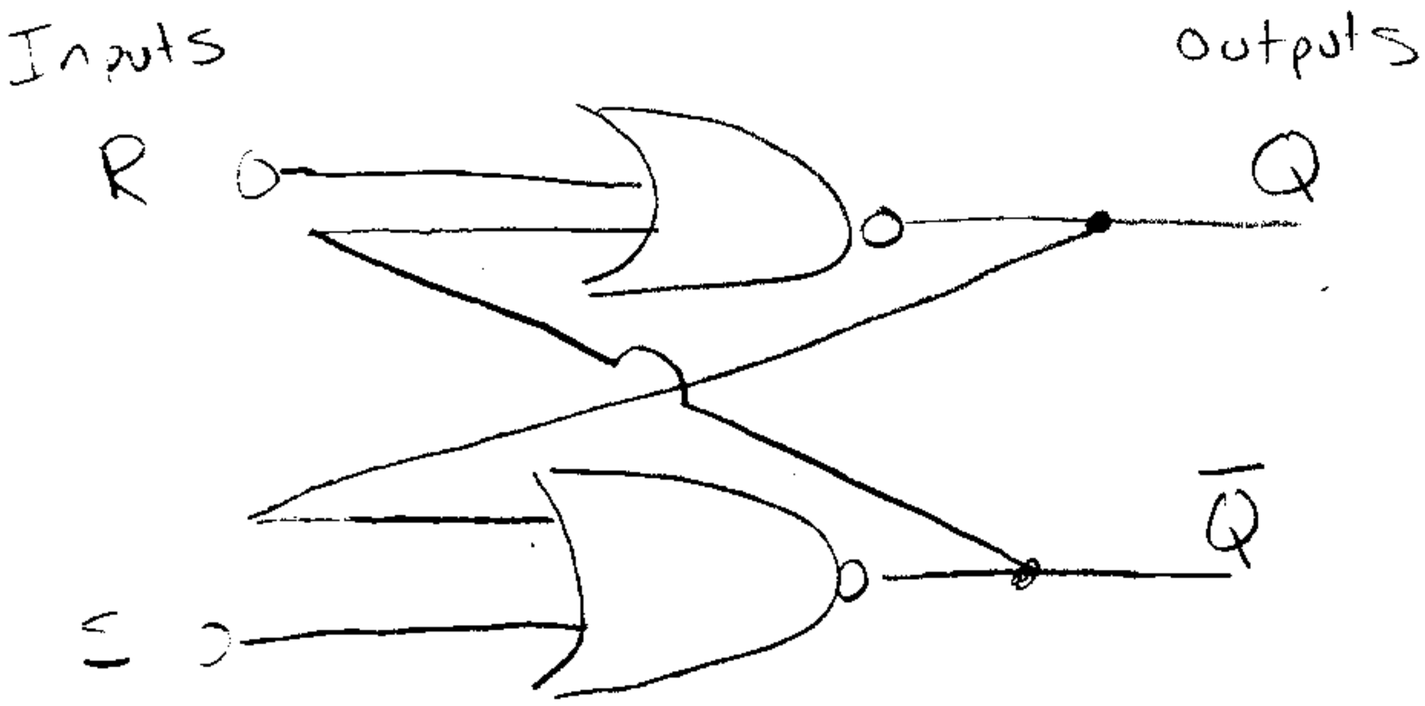
Lecture 23

Memory Elements: Flip-Flops, SRAM, and DRAM

We have now looked at circuits that compute with voltages and analyzed this computation in detail. We have looked at combinatorial circuits.

We now need to find a way to store voltages, so we can sequence our computations.

R-S Flip-Flop



R	S	Q_n
0	0	Q_{n-1}
0	1	1
1	0	0
1	1	not used

This circuit uses feedback. The output is fed back into the NOR input. So the output at any step n depends on the output at step n-1 as well as the inputs R and S. Steps are controlled by a clock, to be shown.

This circoit "stores" a bit.

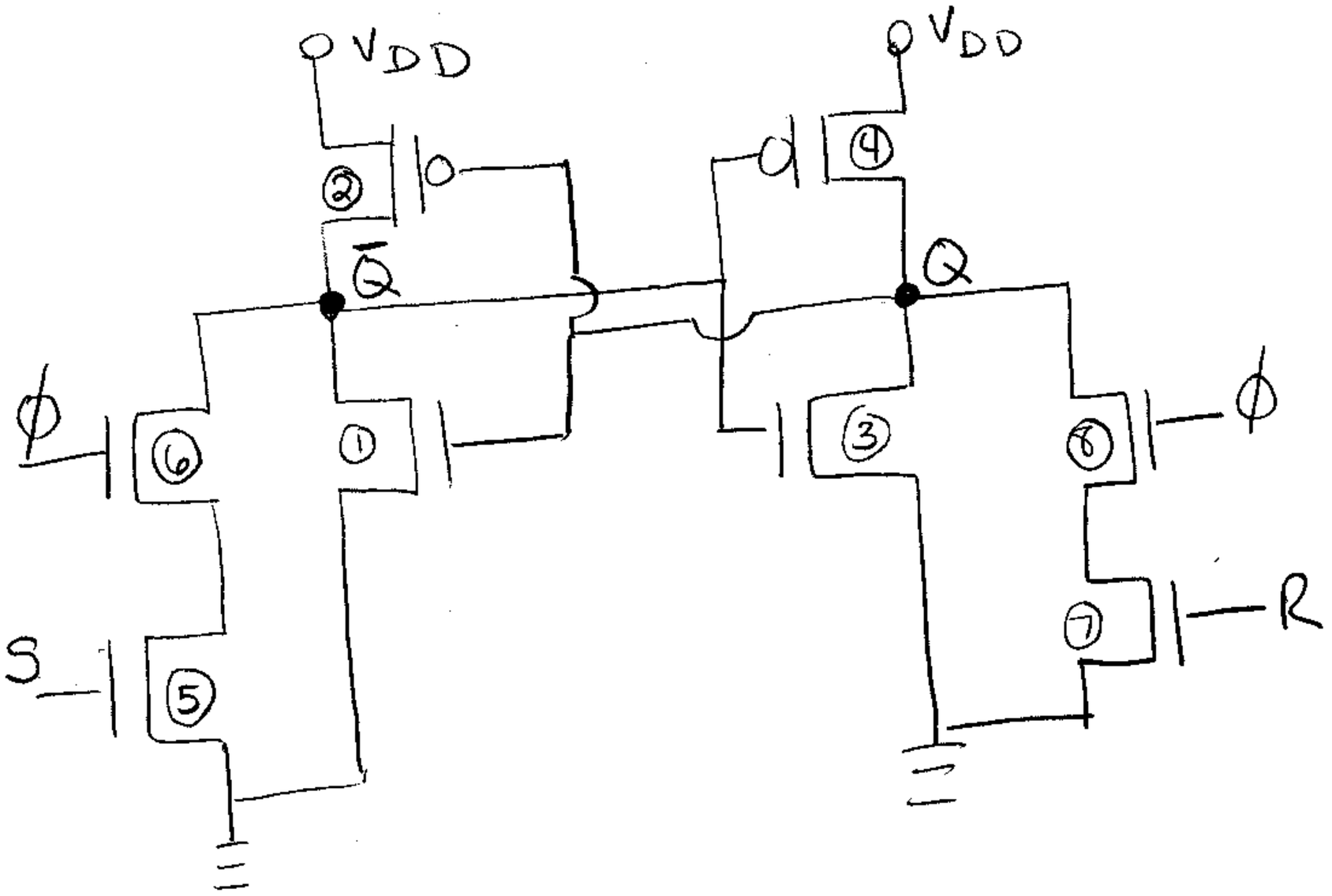
Apply R=1 (S=0) to write a "0".

Apply S=1 (R=0) to write a "1".

Apply R=0 S=0 for no change, just maintaining the previous output.

We call the output Q the "state".

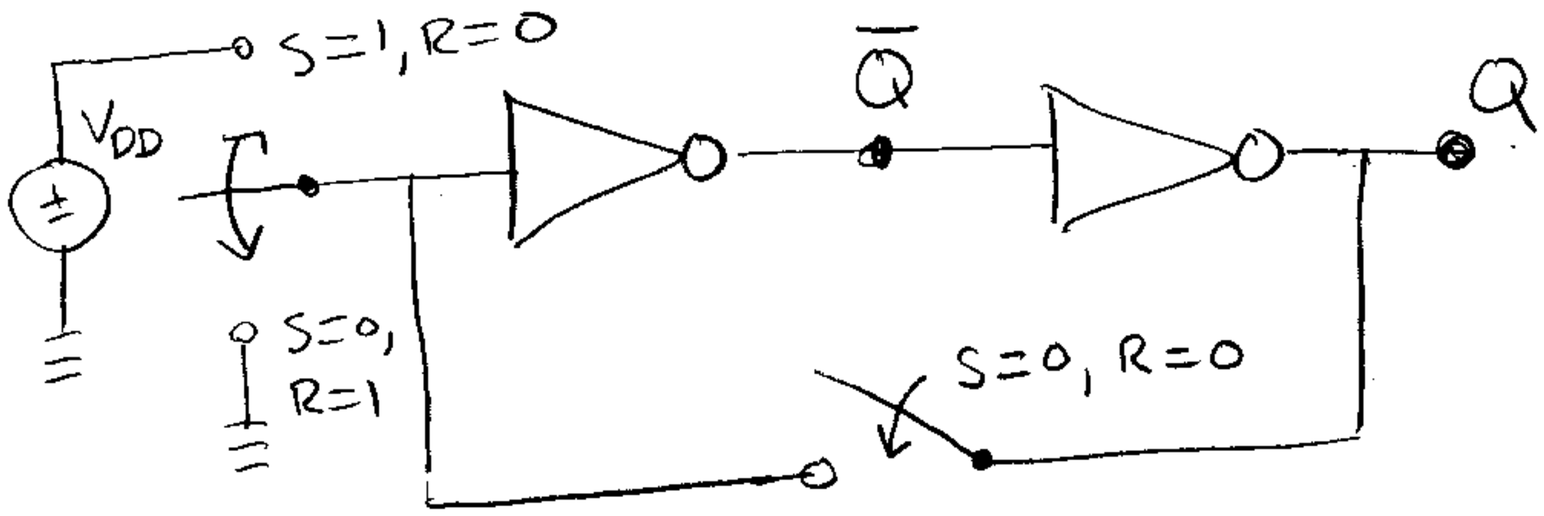
Inside the R-S flip-flop:



ϕ is the clock signal.

Notice that this doesn't really look like two CMOS NOR gates once we go inside.

It looks and functions more like:



Switches move simultaneously at clock ticks.

As long as ϕ is low, ⑥ and ⑧ are open circuits. No new input to the inverters, everything stays the same as before. Input essentially disconnected.

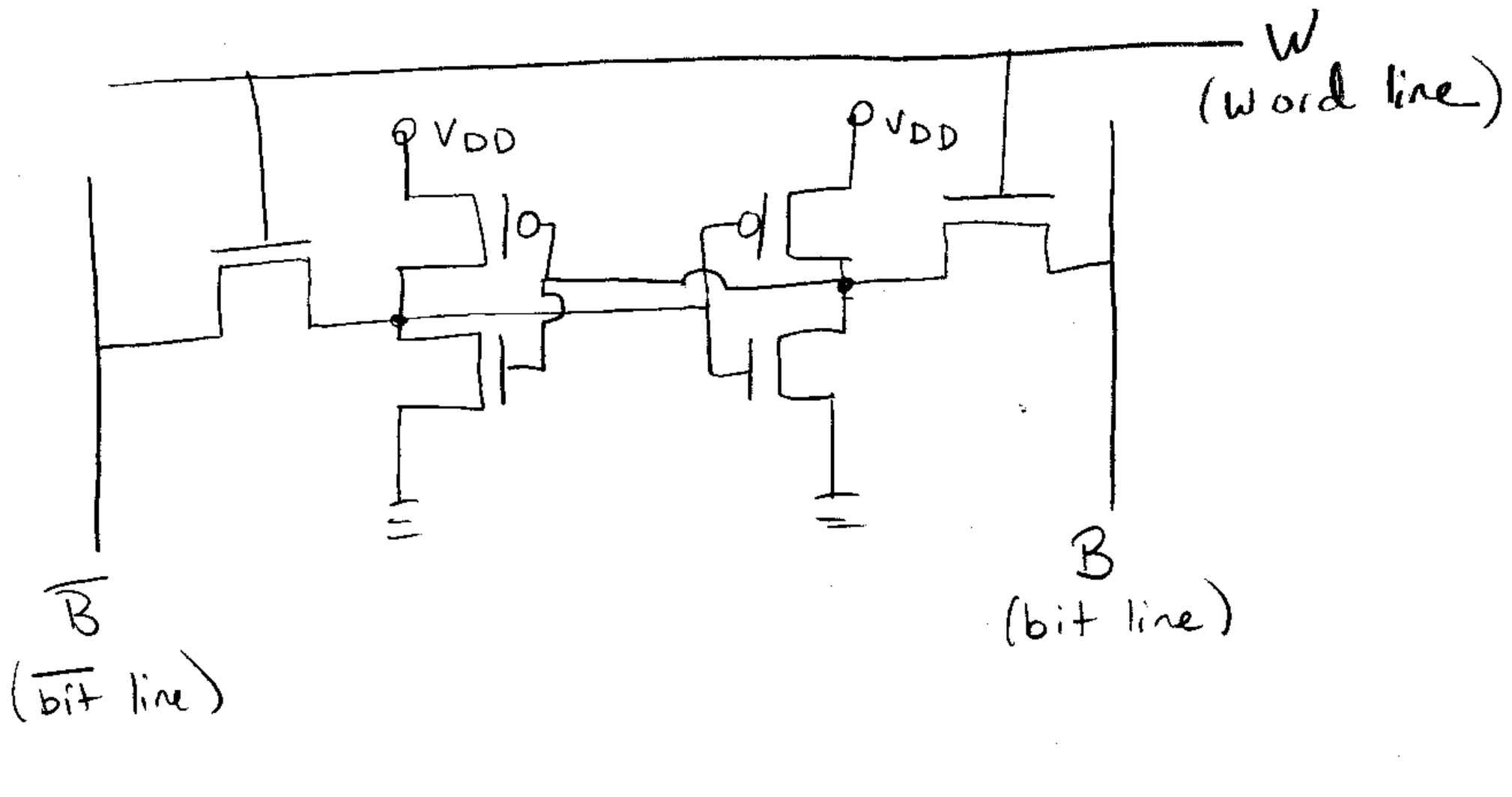
When ϕ goes high, there is now a connection between the inverter inputs and ⑤ and ⑦. Suppose S=1 and R=0. Then ⑦ is open circuit. If $\overline{Q}$ is currently zero (Q=1) then V_{DS} for ⑤ and ⑥ are zero. No current flow, no change. But if $\overline{Q}$ is high, V_{DS} for ⑤ & ⑥ will be nonzero and current must flow down ⑤ & ⑥. This discharges the gates of ③ & ④. the voltage at the gates goes down. $\overline{Q}$ goes down. Q, being the inverter output, goes up. This pushes $\overline{Q}$ down

further since it too is an inverter output.
This positive feedback drives Q to V_{DD} and $\overline{Q}$ to 0.
The opposite occurs when R=1 and S=0.

This is our static memory element.
The flip-flop keeps the same state (stores the bit) forever until you change it.
Other digital circuits can use Q (read the bit) without changing the stored voltage.

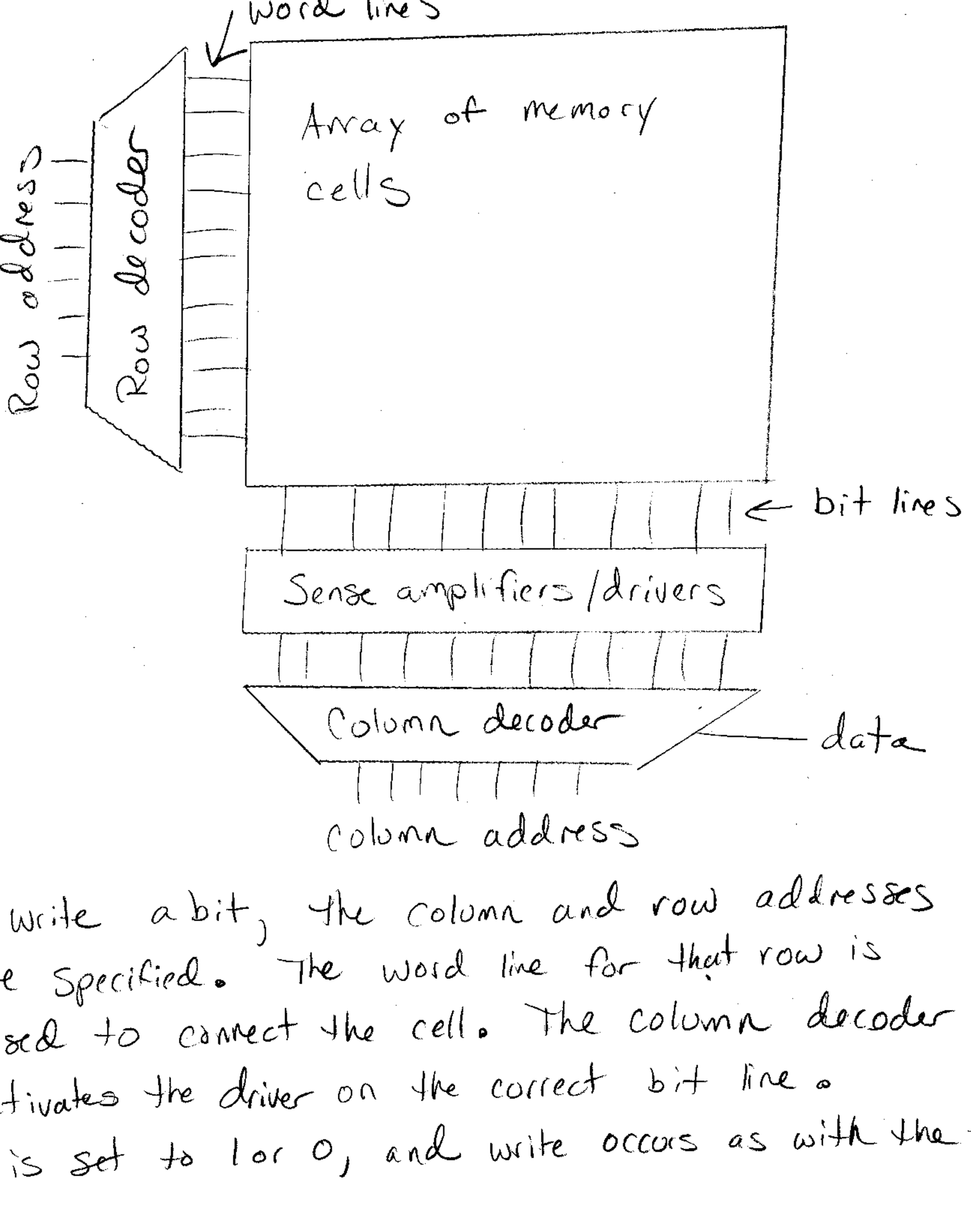
SRAM (Static Random-Access Memory)

The following, slightly simpler cell is often used to store a bit in SRAM:



When W is low, the cell is isolated and stores its bit.

When W is high, the cell is connected to the bit lines and can be read or written.



To write a bit, the column and row addresses are specified. The word line for that row is raised to connect the cell. The column decoder activates the driver on the correct bit line. B is set to 1 or 0, and write occurs as with the flip-flop.

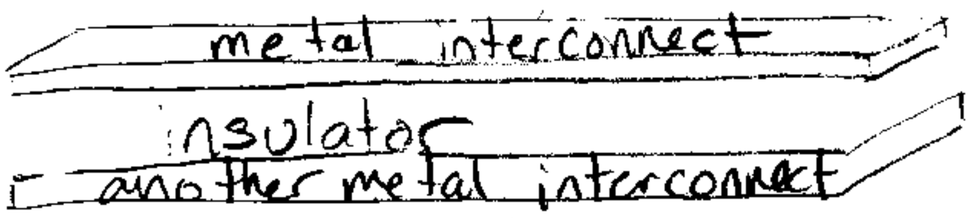
The read operation is a bit trickier, since the same line B is used for both read and write.

We want B to change to detect the state of the cell, but not so much that the state of the cell gets changed in the process. So we:

- Precharge B and $\overline{B}$ to $V_{DD}/2$.
- Set W to V_{DD}.
- Wait for B + $\overline{B}$ to change.

  We only need to wait until B changes by about 0.1 V. The sense amplifier will detect whether we are headed towards 1 or 0. The cell must be made so that charging B does not change the state.
- Output of sense amplifier is the read data.

Why do we say we need to "charge" the bit line? It is a wire, not a capacitor...



Semiconductor circuits are layered (note all our 3-D jumps).

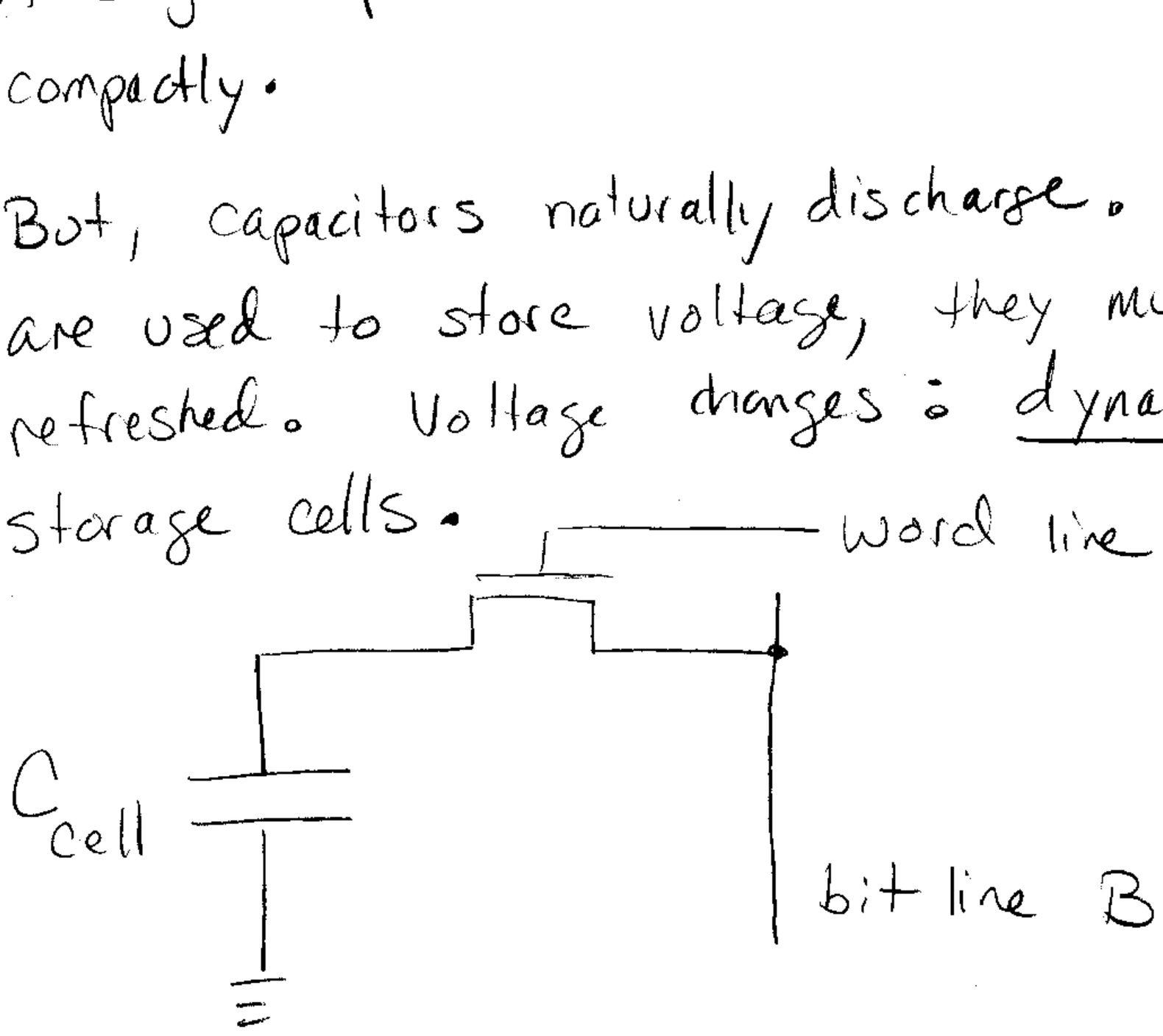
Wires definitely have capacitance & require charging.

DRAM (Dynamic Read-Only Memory)

SRAM cells have at least 6 transistors apiece.

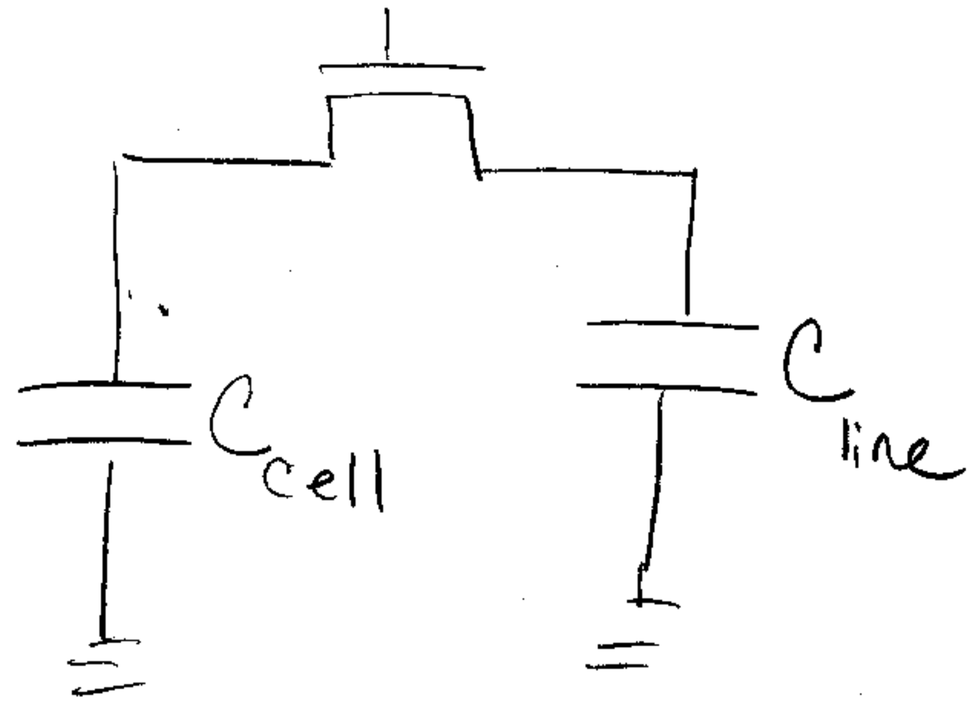
A single capacitor can store a voltage - much more compactly.

But, capacitors naturally discharge. If they are used to store voltage, they must be refreshed. Voltage changes : dynamic storage cells.



When W is high, we can write to the cell by holding B high or low. Capacitor will charge or discharge.

To read, C_{cell} shares its charge with the bit line capacitance. Typically, C_{line} is bigger than C_{cell}, so



C_{cell} would have to give more than half its charge to equalize the voltages.

A sense amplifier detects early on whether B is being charged to logic 1.

The sense amplifier refreshes both of the capacitances if this is the case.

Reads & writes refresh C_{cell}, but we don't want an unused cell to just degrade. Periodically, the cells are all refreshed, row by row in a "burst". This means reads & writes are unavailable about 2% of the time.

Example:

Suppose C_{cell} is charged to 4 V and C_{line} is charged to 0 V at $t=0$.

At this time, W goes high and the transistor turns into a 1KΩ resistor.

At what time will the voltage on C line equal 0.2 V (so the sense amplifier can detect it)?

Use $C_{cell} = 10_{pF}$ and $C_{line} = 100_{pF}$.