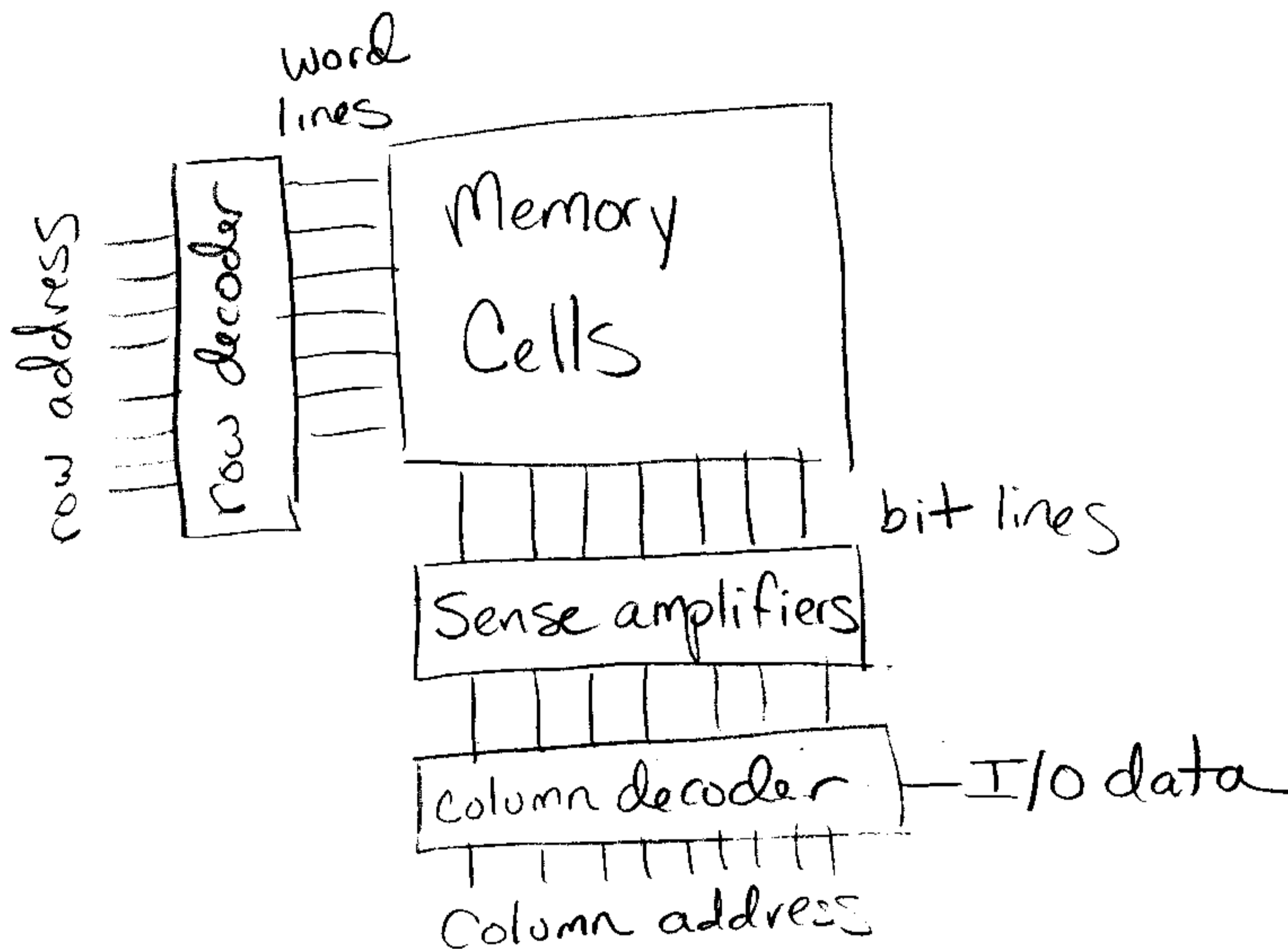


## Lecture 24

### MOS Memories: Sense Amplifiers, Address Decoders, and ROM



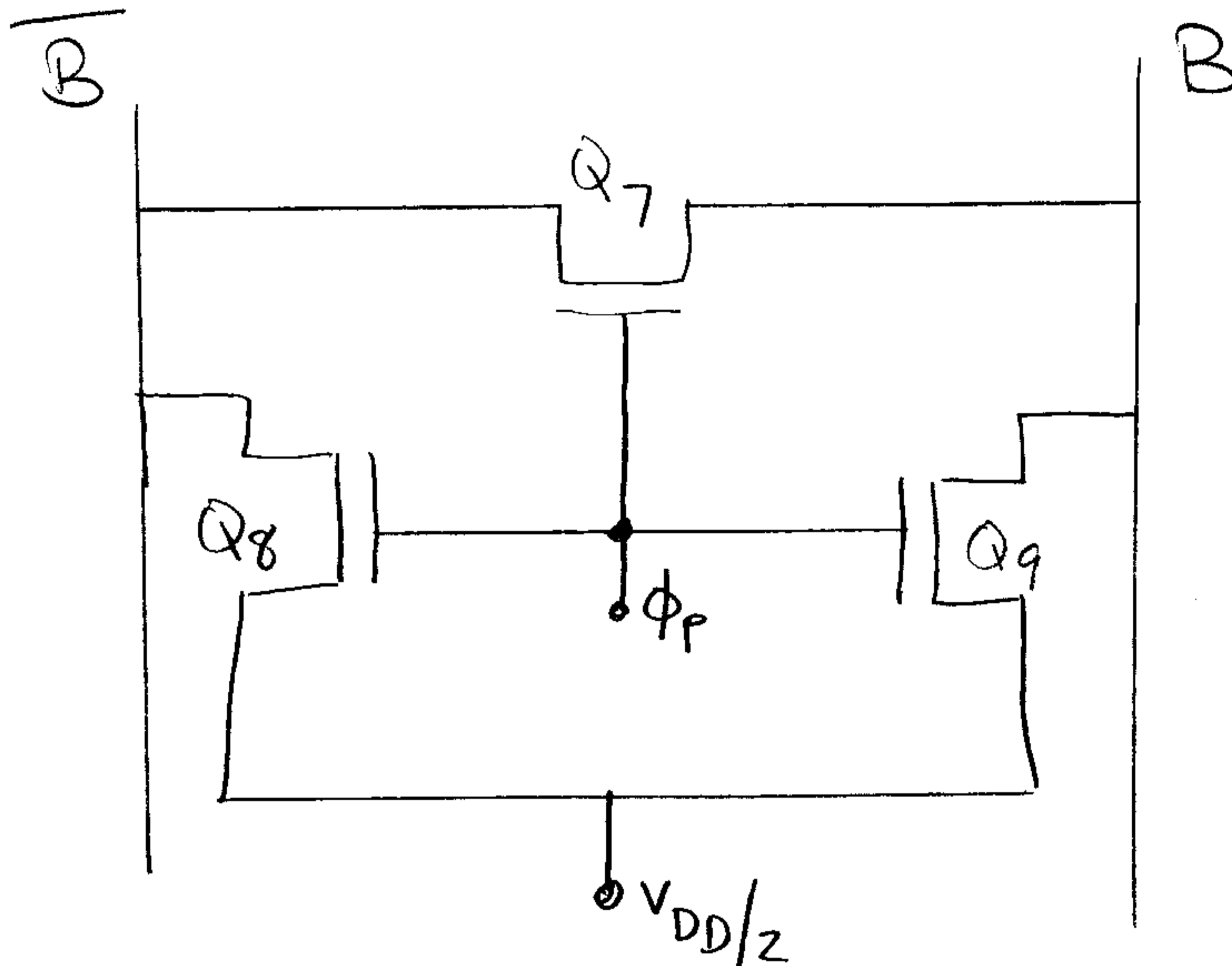
Last time we investigated SRAM and DRAM memories.

We needed an address decoder to select the column and row where our desired data lies.

We used sense amplifiers to see early on if a 1 or 0 was being read, so that our reads would be non-destructive (the act of reading would not discharge the memory cell).

Before reading, we precharged the bit line to  $V_{DD}/2$  so we could then connect the memory cell to read and see if the bit line voltage went up or down. We need a circuit to do this precharging.

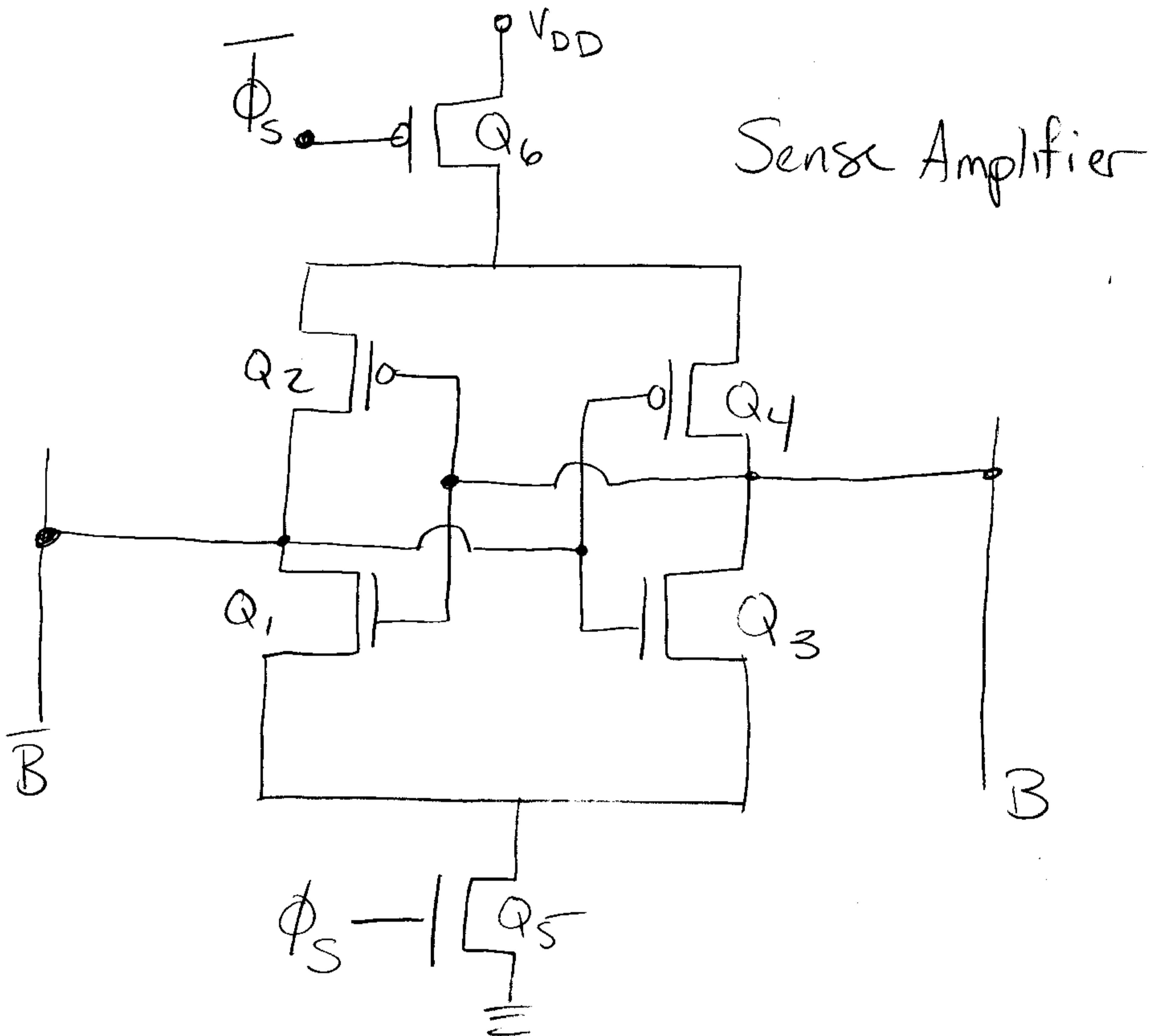
## Precharge Circuit



To precharge the B and NOT B lines to  $V_{DD}/2$  before reading,

- The signal  $\Phi_p$  is set high.
- All three transistors conduct.  $Q_8$  and  $Q_9$  act as resistances connecting B and NOT B lines (which act as capacitors) to  $V_{DD}/2$ .
- $Q_7$  speeds up the process by helping equalize the two voltages.
- Note that these are special NMOS transistors which can conduct current in either direction, so they can both charge and discharge the lines.
- The signal  $\Phi_p$  goes low when charging is complete.

## Sense Amplifier with SRAM

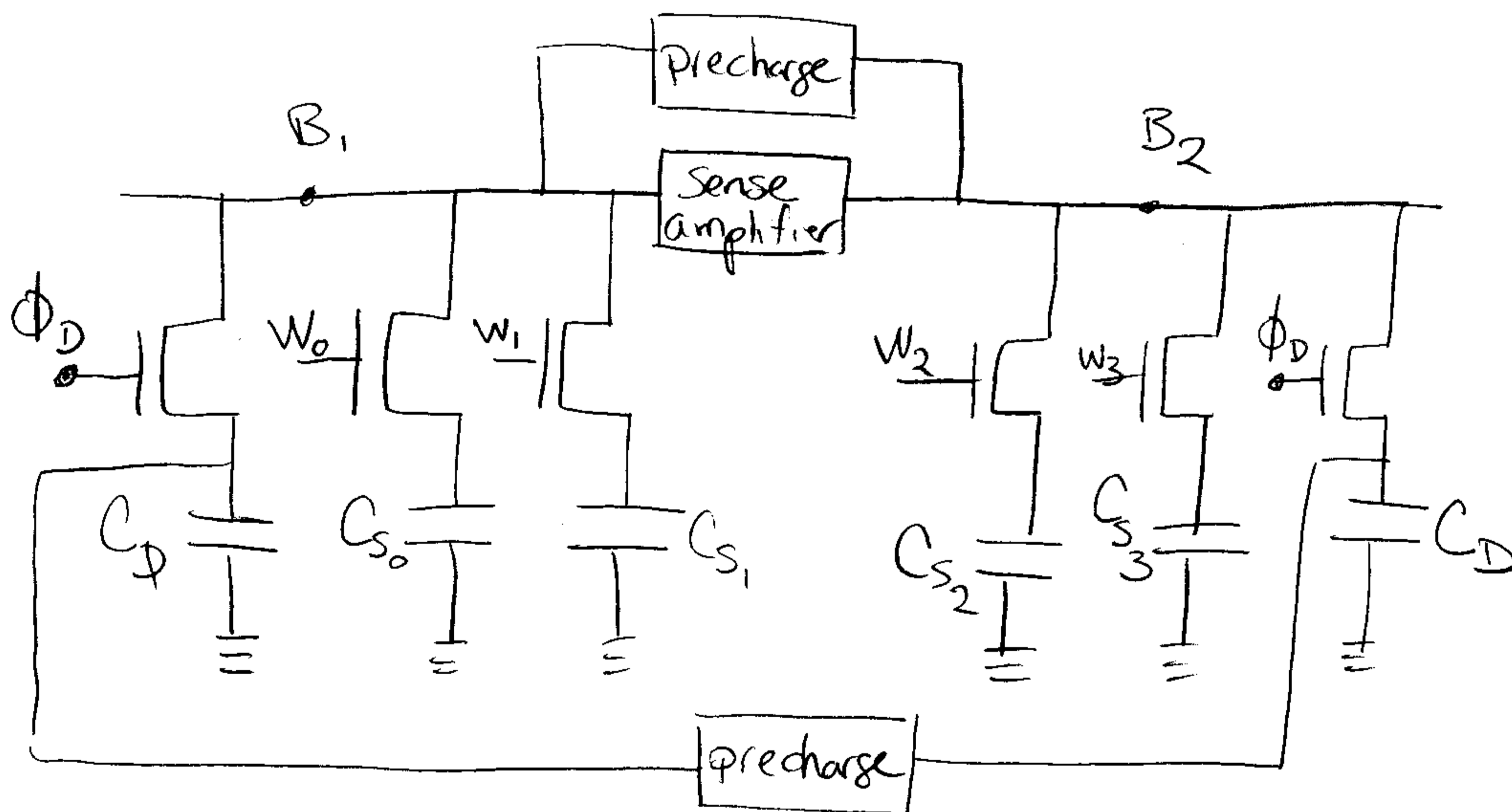


The sense amplifier is best described not as an amplifier, but a positive feedback device that quickly pushes the readout voltage to 1 or 0.

The sense amplifier assists (and basically takes over) the charging of the  $B$  and  $\text{NOT } B$  lines so that the memory cell doesn't discharge and lose its data.

- When  $W$  goes high and the read begins, the memory cell will begin to charge/discharge the  $B$  and NOT  $B$  lines.
- Shortly after the read begins,  $\Phi_s$  goes high to activate the sense amplifier (connect it to  $V_{DD}$  and ground).
- The positive feedback of the sense amplifier will quickly drive the lower line to  $0\text{ V}$  and the higher line to  $V_{DD}$ , essentially by repeated inversion of the voltages.
- The sense amplifier provides the charges necessary to change the voltage of the  $B$  and NOT  $B$  lines, so the gates of the SRAM cell are not discharged so as to corrupt the data.

### Sense Amplifier with DRAM



The sense amplifier can be used with DRAM, if we can come up with a NOT  $B$  line for the DRAM cell. We do this by dividing the bit line in half, and adding two "dummy cells" on the ends.

- The two halves of the bit lines are first charged to  $V_{DD}/2$ .
- The capacitors  $C_D$  are also charged to  $V_{DD}/2$ , by holding  $\Phi_D$  high.
- The charging signals go low when charging is complete.
- The word line on one of the cells goes high to start the read.
- $\Phi_D$  for the dummy cell on the opposite side is set high.
- The selected DRAM cell begins to charge or discharge its half of the bit line.
- The voltage on the other half of the bit line stays at  $V_{DD}/2$ , since the dummy capacitor it is connected to is also at  $V_{DD}/2$ .
- After a short time, the sense amplifier is activated.
- The bit line with voltage  $V_{DD}/2$  will not cause the sense amplifier to drive the bit lines to 1 or 0, but the bit line of the selected DRAM cell, being slightly above or below  $V_{DD}/2$  will trigger the feedback. The selected cell's half of the bit line will be driven to 1 or 0, the contents of the DRAM cell. The other half will be driven in the other direction.
- Additional logic selects the "correct" half of the bit line for the output.

Once again, the sense amplifier acts as a driver, supplying the charge to bring the bit line to the correct level, so that the DRAM capacitor's stored charge is not drastically affected.

The driving process also restores (refreshes) the voltage on the DRAM capacitor.

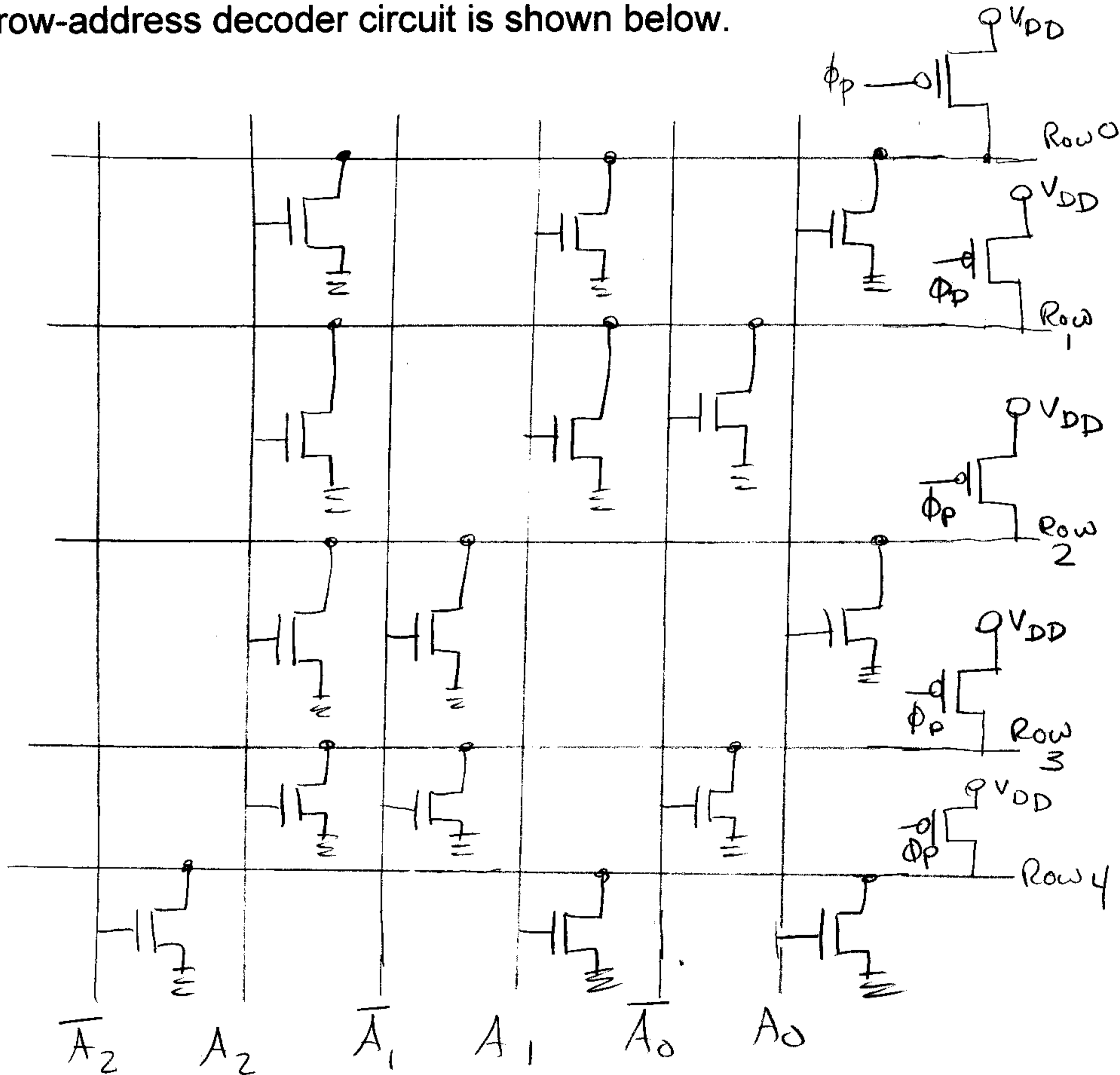
## Row-Address Decoder

The row-address decoder needs to activate the right word line, depending on the address input.

For example, for a 3-bit address  $A_2, A_1, A_0$ ,

Row 0 is selected if  $\bar{A}_2\bar{A}_1\bar{A}_0 = 1$  and Row 5 is selected if  $A_2\bar{A}_1A_0 = 1$ .

A row-address decoder circuit is shown below.

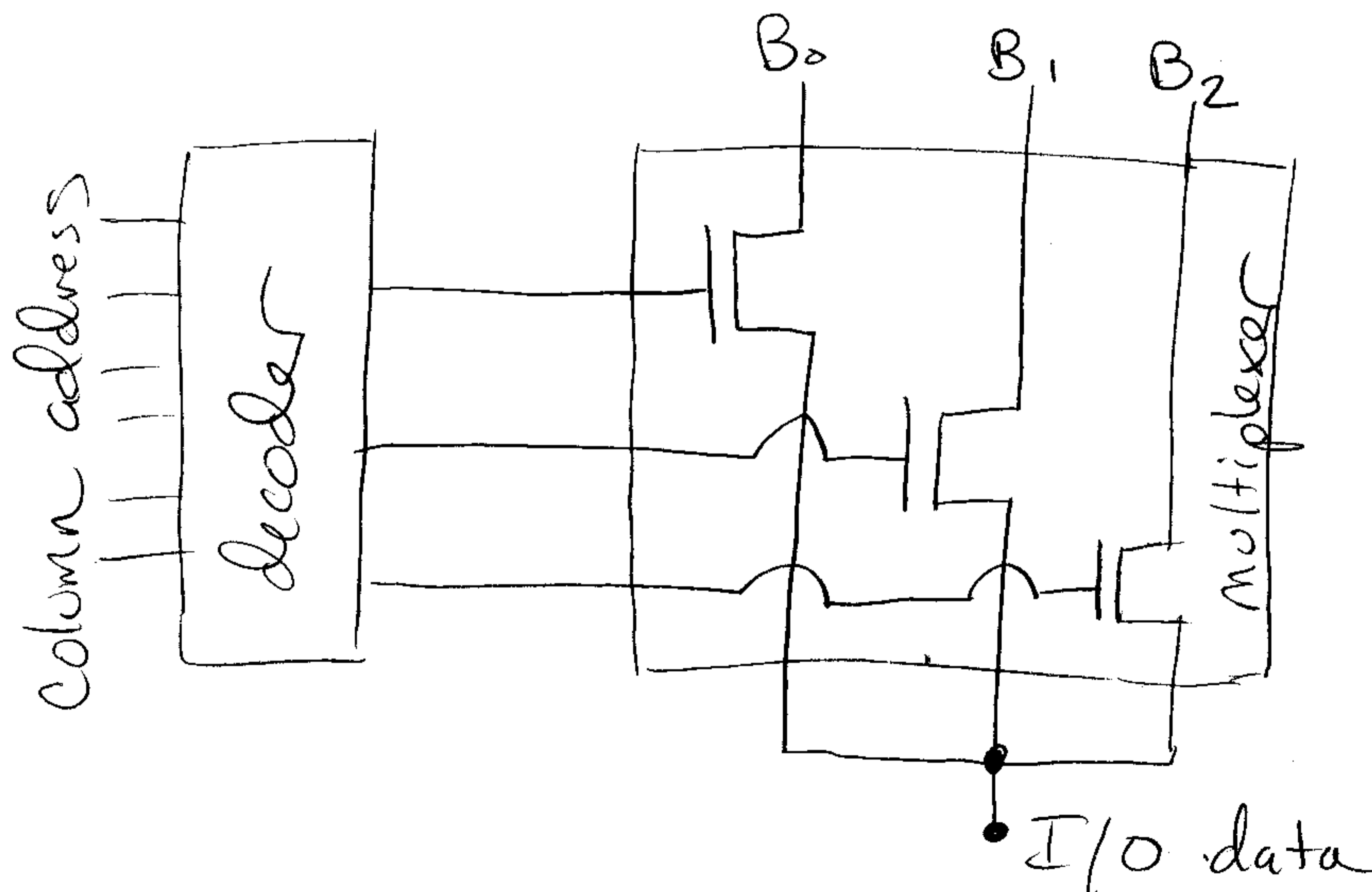


- Before decoding, all rows (word lines) are precharged to  $V_{DD}$  by setting the signal  $\Phi_p$  high to make the PMOS conduct, and all address inputs low to make the NMOS open.
- Then the signal  $\Phi_p$  goes low, and the row address is applied.
- Only one row will have all three NMOS turned off. This row will stay charged at  $V_{DD}$  since there will be no discharge path.
- The rest of the rows have at least one NMOS conducting, and connecting the row to ground. These rows will discharge.

### Column-Address Decoder

This circuit is very similar to the row decoder, but it is a multiplexer—it must select a bit line to connect to the I/O line based on the column address.

Here, the decoder turns on the correct transistor, forming a conducting path from the correct bit line to the I/O line.



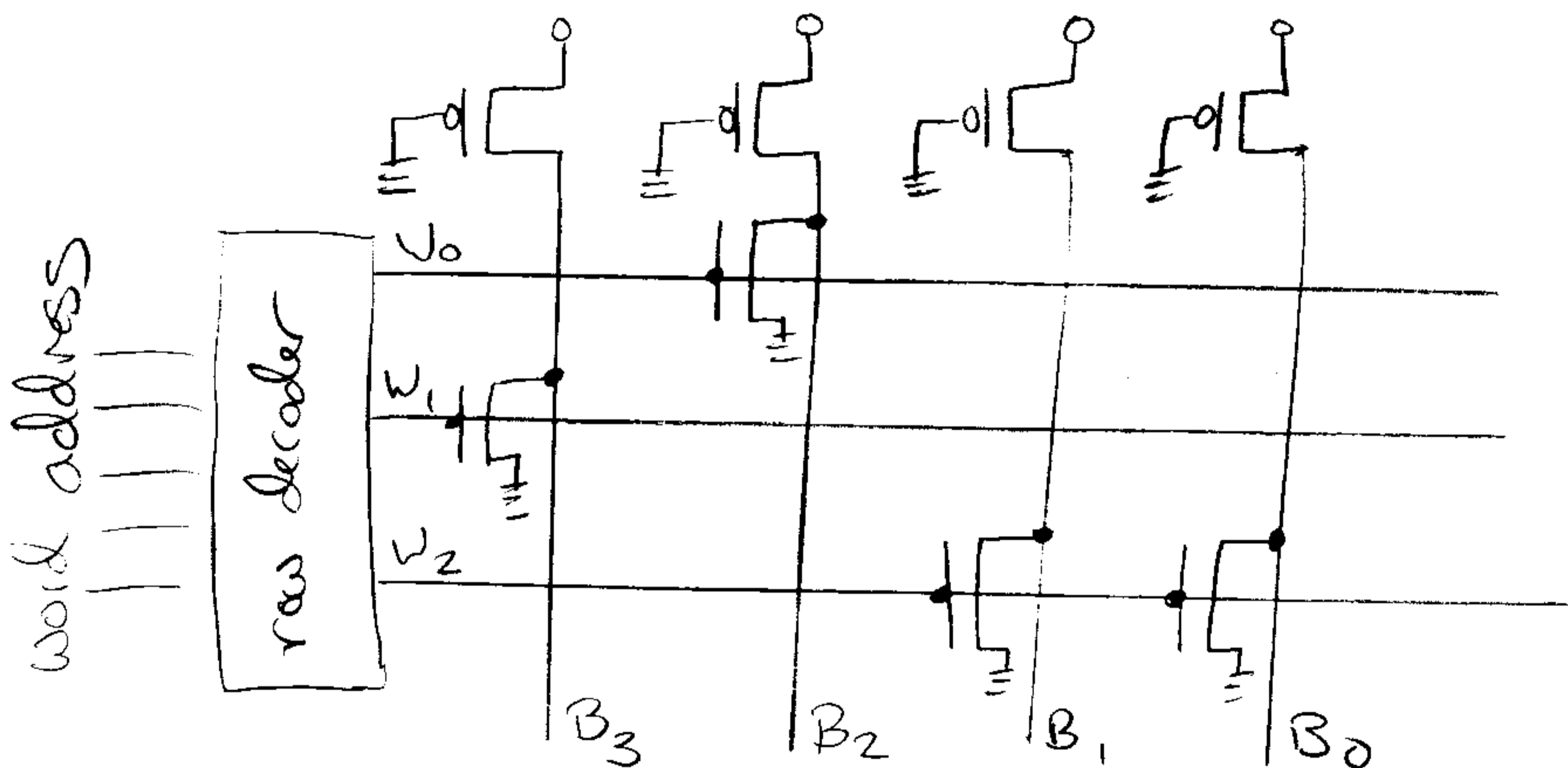


## ROM (Read-Only Memory)

There are several ways to create ROMs. We will look at one way to do this using the NMOS transistors we learned about: **the mask-programmable ROM.**

A silicon wafer is made with an array of NMOS transistors, with sources at ground and drains connected via a grid of aluminum.

The ROM is written by etching away the aluminum drain connection for each cell where a 1 should be stored, yielding a circuit like this:



Before a word is selected, all bit lines are high due to the conducting PMOS which is attached to  $V_{DD}$  on the top of the circuit.

When a word is selected, the NMOS in that row are turned on and conduct. Wherever there is an NMOS, the bit line voltage will go down. The sense amplifier will bring these bit lines to 0 V. The lines without an NMOS stay at  $V_{DD}$ .

This might seem like a waste of transistors, since many are disconnected, but customization at the transistor level is more expensive since fabricator time is so valuable.