Lecture 25

Oscillator, Counter, and A/D Converter

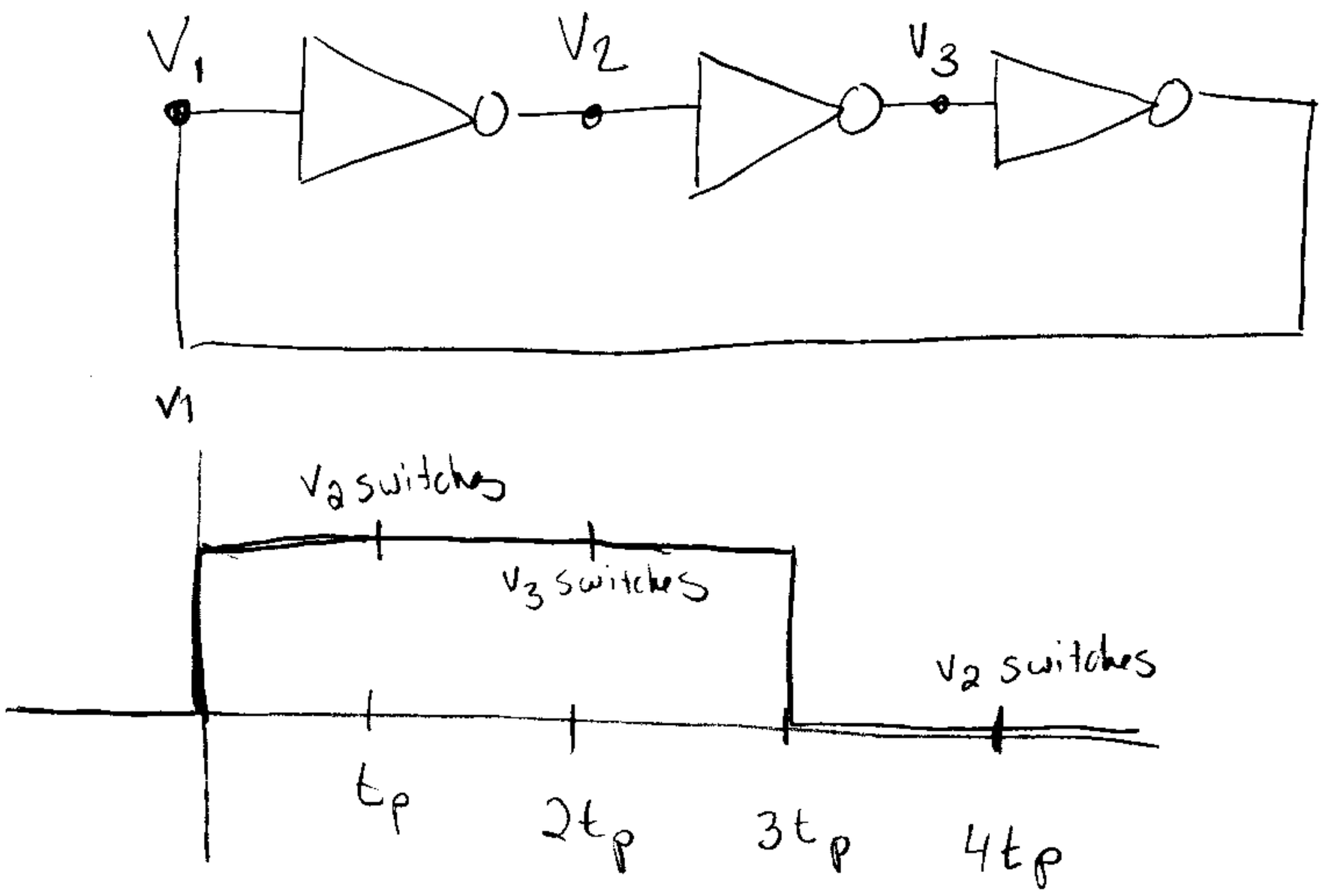
Today we will learn how to create a clock signal—using the **ring oscillator**.

We will learn how to change the frequency of the clock using a **ripple counter** (which is also useful for counting).

We will use both of these circuit to make **analog-to-digital converters**. We made a 2-bit A/D converter in homework, and today we will learn about some common implementations of larger-scale A/D converters.

Ring Oscillator

Suppose we connect an **odd** number of inverters in a loop:



The voltage at any point will invert every n t_p seconds, where n is the number of inverters.

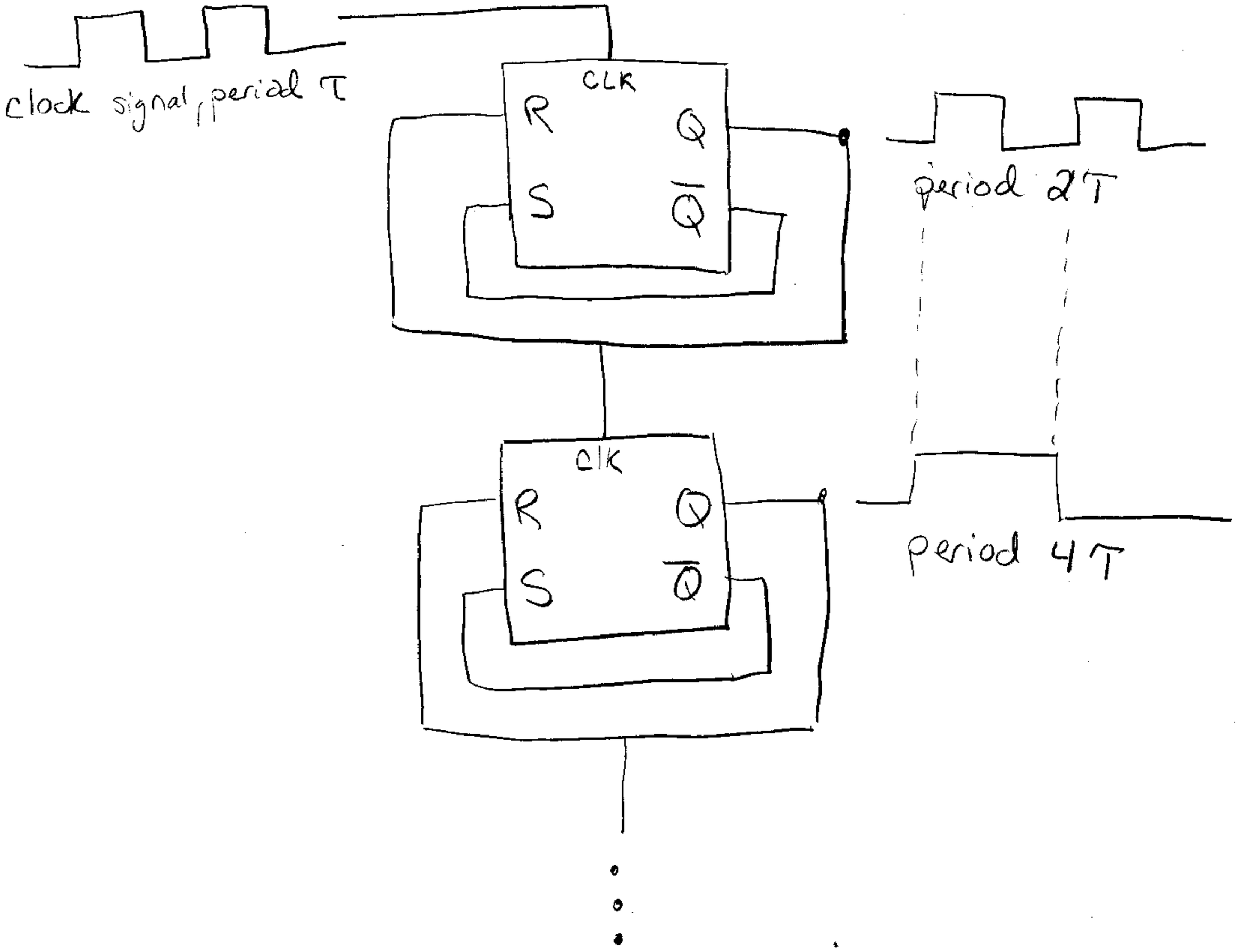
We can create a clock signal this way!

Ripple Counter

We can change the frequency of our clock signal by adding more inverters in the oscillator. But, if we want a low frequency (high period) signal, this will take a lot of inverters!

We can use flip-flops to implement a circuit that counts clock ticks. The higher place values in the counter will have lower frequency.

Assume that the flip-flops below are positive edge triggered (changes occur as the input clock signal rises).



Each output signal serves as a clock input to the next flip-flop. One entire period (positive edge to positive edge) of a given flip-flop output corresponds to one half-period (one transition) of the next flip-flop. The circuit thus counts ~~up~~ down in binary. Count up - negative edge triggers

A/D Converters

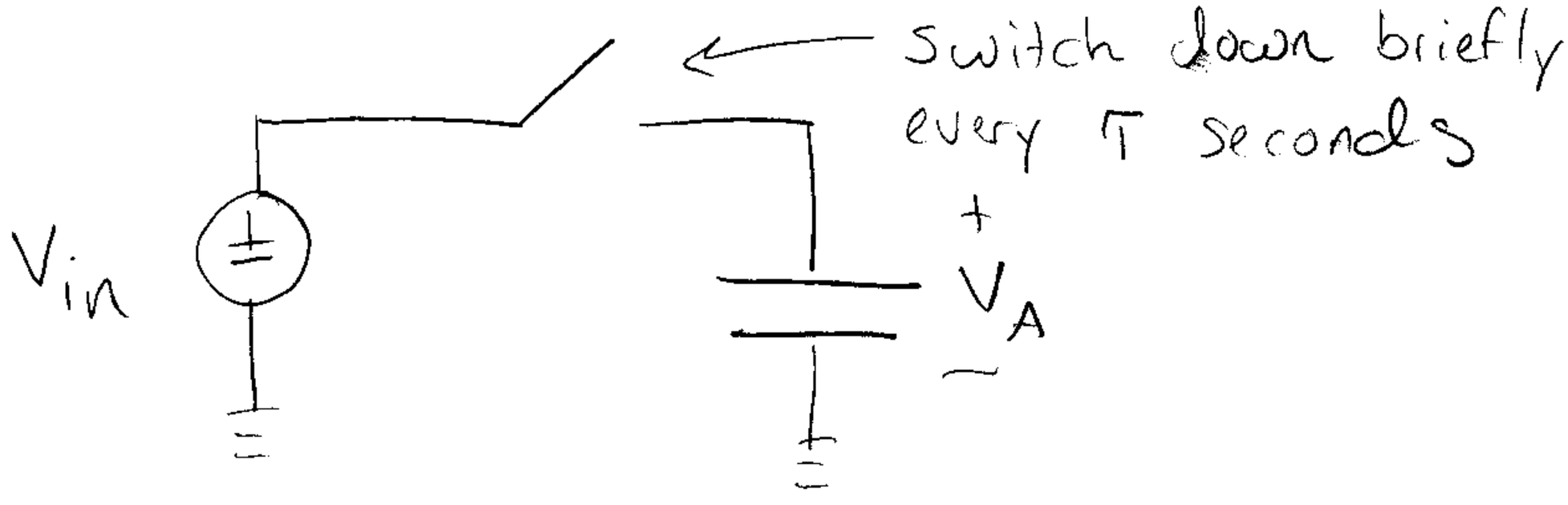
When we studied op-amps and comparators, we came up with circuits for D/A conversion and A/D conversion. Our D/A conversion circuit is the standard circuit used for this purpose. We will now explore several common circuits used for A/D conversion.

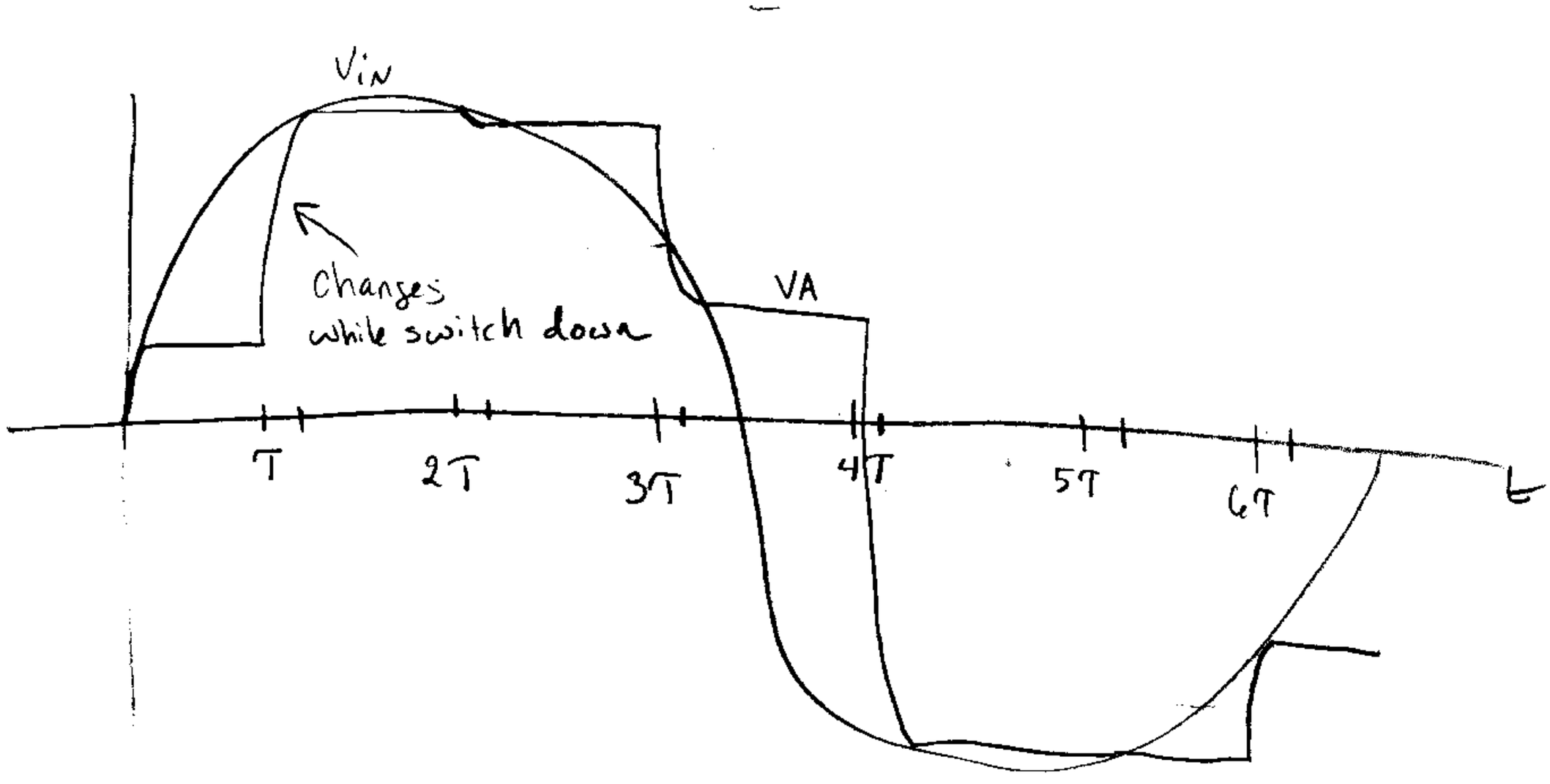
Sample-and-Hold

The first step in A/D conversion is to sample the signal. We take the value of an analog input every τ seconds, and hold it constant for τ seconds.

This can be accomplished by the circuit below. The switch shown can be implemented using an transistor that we turn on and off. For fast response, we want the capacitance and transistor resistance to be small.

The output, which is mostly constant over τ second intervals, can be fed to a variety of different circuits for conversion.

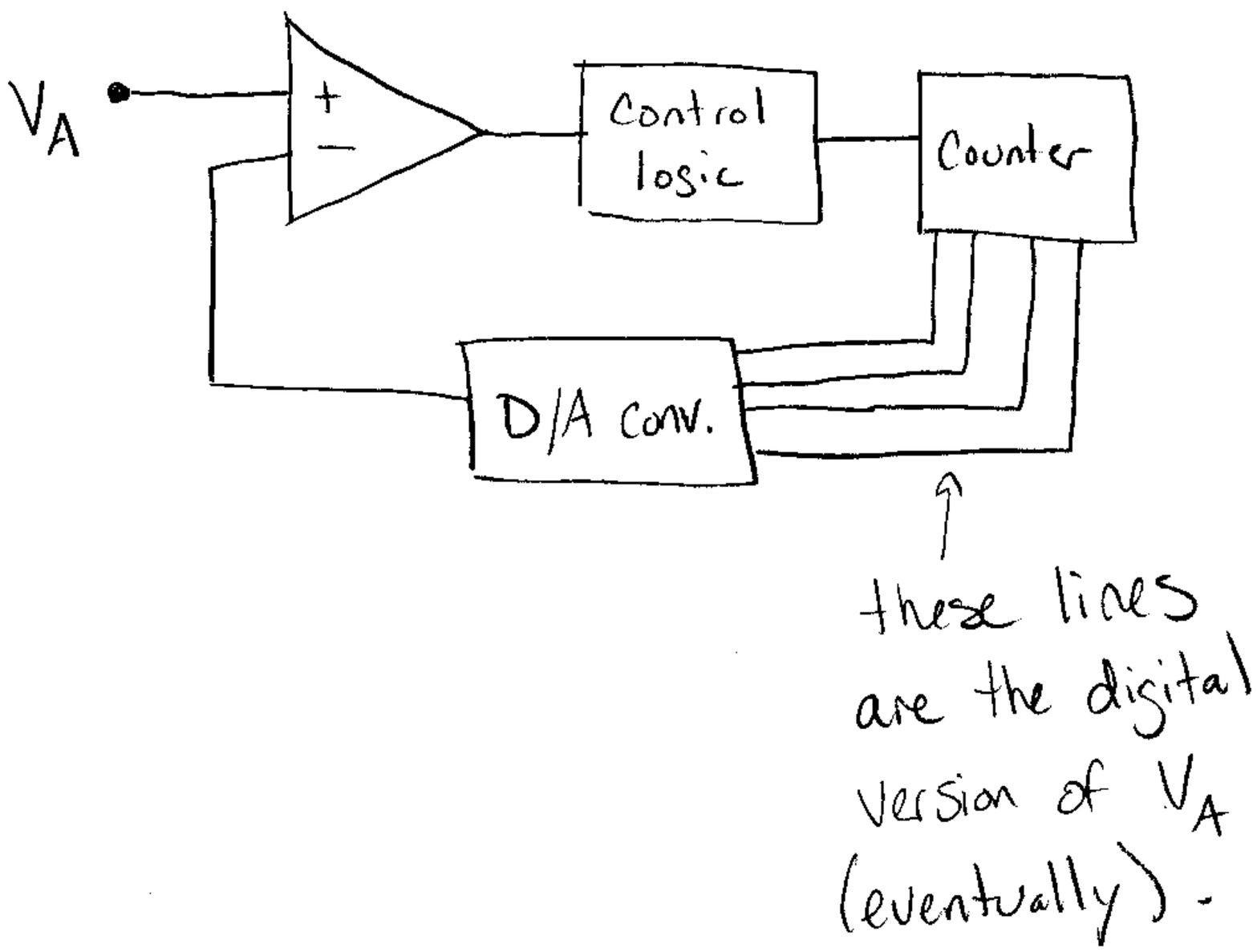




Feedback A/D Converter

The A/D converter below takes our "staircase" analog signal and compares it to a value stored in a counter (converted to analog so we compare apples to apples!). If the input signal is higher then the counter value, it counts up. If lower, the counter counts down. It continues counting until the situation changes (when the counter crosses the value of the input signal). Then it stops counting, and the value on the counter is the digital value of the input.

The counting had better be fast, since it needs to converge to the correct value while the input is held constant.

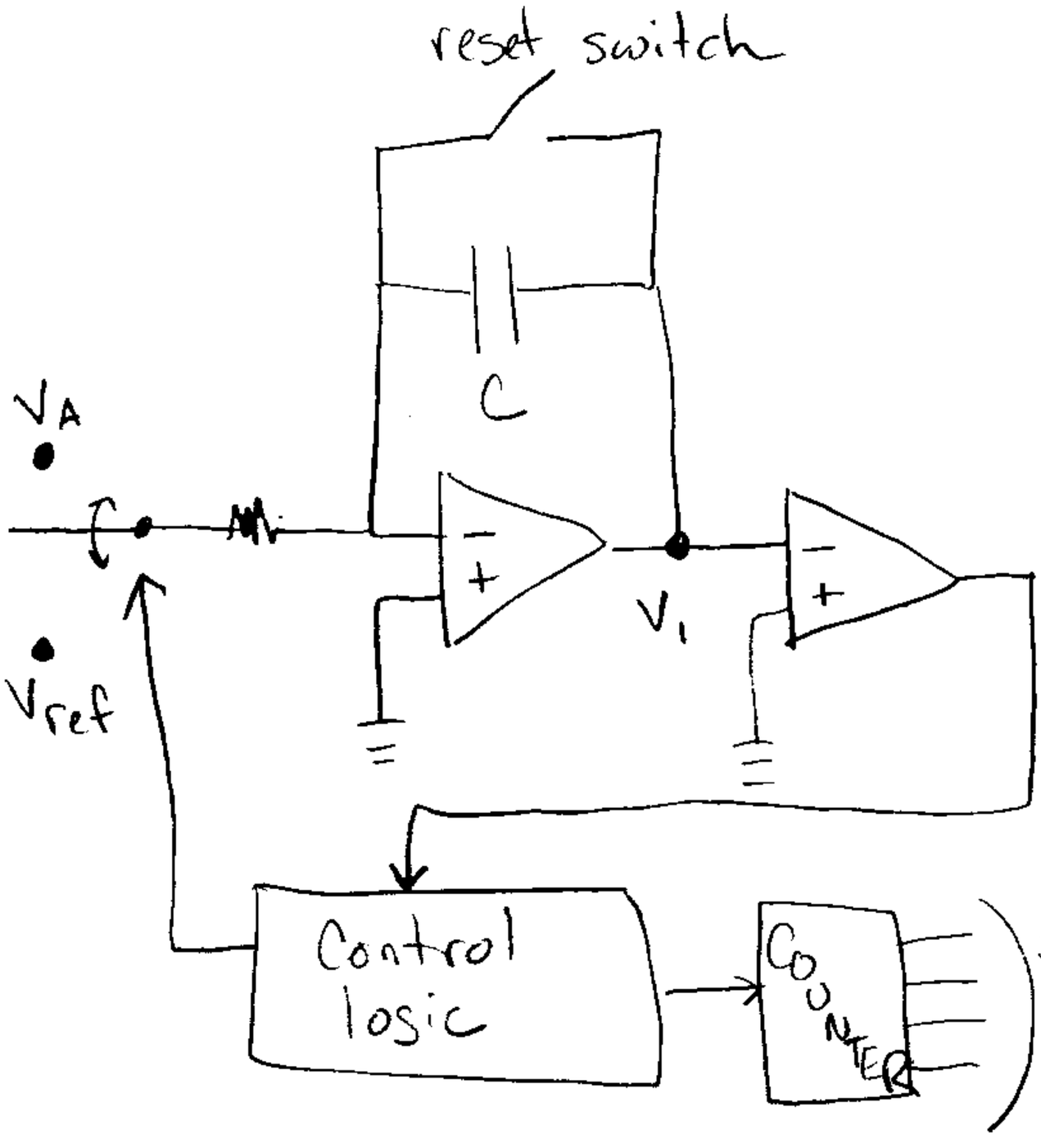


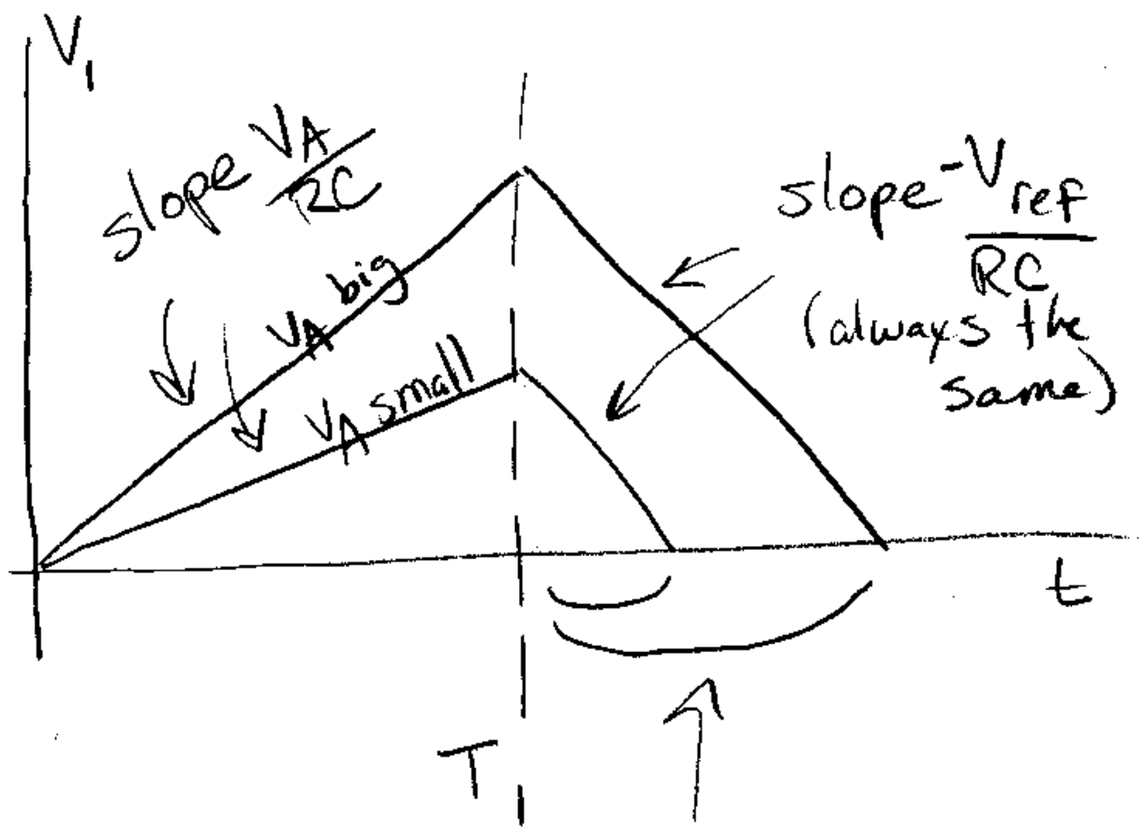
Dual-Slope A/D Converter

This circuit integrates the analog input signal v_A over part of the interval in which it is held constant. Suppose it integrates from time 0 to T_1. The value at the output of the integrator, since the input is constant, will be $v_1 = -(v_A)(T_1)(RC)$. Note that the picture below is drawn for negative v_A.

At time T_1, the input to the integrator is changed to a constant reference voltage V_{ref}, with sign opposite that of v_A. Integration continues until the output of the integrator hits zero. The counter measures how long this takes. Suppose that the counter reads n when it stops.

Suppose that the maximum value that the counter can display is n_{ref}, and that $-V_{ref}$ represents the largest-magnitude analog voltage on our scale (corresponding to the digital value n_{ref}). It can be shown that $n = n_{ref}\left(\frac{v_A}{V_{ref}}\right)$ so the circuit indeed provides the digital equivalent of v_A for the given voltage scale.





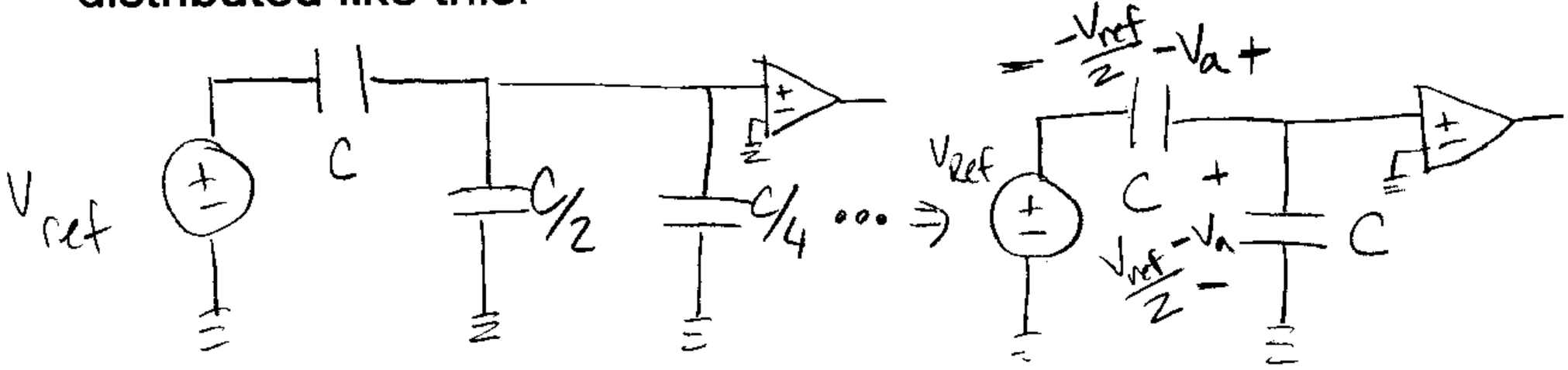
the bigger V_A is, the more time it takes to get back to 0 V ⇒ bigger counter value.

Counter value proportional to V_A with max corresponding to V_{ref}.

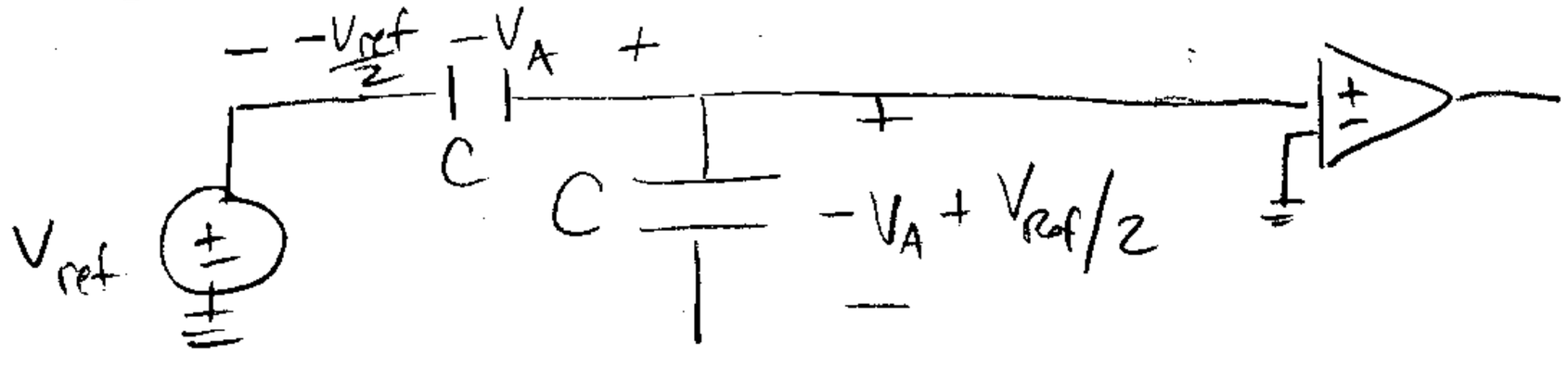
Charge-Redistribution A/D Converter

The circuit below operates in the following manner:

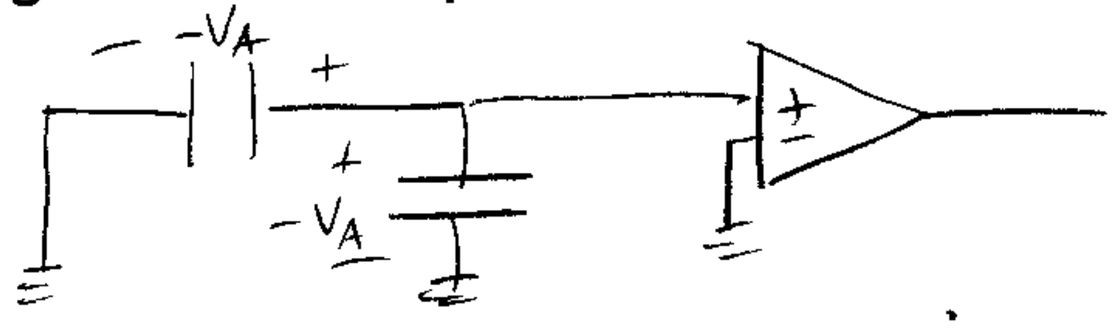
1. All capacitors are charged to vA on their **bottom** plates, with top plates grounded. See diagram (a) on the next page.
2. The capacitors are disconnected, having been charged to vA on the bottom. See diagram (b) on the next page.
3. The largest capacitor, C, is connected to V_{ref}, which represents the maximum voltage on the scale. The rest of the capacitors combine in parallel to form another capacitor of capacitance C. The charge is distributed like this:



4. The comparator checks whether the voltage over the capacitor is negative ($v_A > V_{ref}/2$) or positive. This tells us what the most significant bit should be. See diagram (c) on the next page.
   a. If negative, the switch for the capacitor stays connected to V_{ref}, so the voltage over the capacitor is $-v_A + V_{ref} / 2$.



   b. If positive, the switch for the capacitor goes back to ground, so the voltage over the capacitor is $-v_A$.



   (In this way, the circuit has subtracted the place value for a "1", and subtracted nothing for a "0").
5. The process is repeated for the rest of the capacitors.
6. The switches on the capacitors at the end of the process tell us which binary place values have "1" and which have "0".