Week 14 Fabrication

OUTLINE

• IC Fabrication Technology
  – Introduction – the task at hand
  – Doping
  – Oxidation
  – Thin-film deposition
  – Lithography
  – Etch
  – Lithography trends
  – Plasma processing
  – Chemical mechanical polishing

Reading (Rabaey et al.)
  • Sections 2.1-2.2
Moore’s Law – Increasing Number of Transistors on a Chip

Transistor count vs. year on Intel computer chips

<table>
<thead>
<tr>
<th>Year</th>
<th>Transistors Per Chip</th>
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<tbody>
<tr>
<td>1972</td>
<td>3,500</td>
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<tr>
<td>1974</td>
<td>6,000</td>
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<tr>
<td>1978</td>
<td>29,000</td>
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<tr>
<td>1982</td>
<td>134,000</td>
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<tr>
<td>1985</td>
<td>275,000</td>
</tr>
<tr>
<td>1989</td>
<td>1,200,000</td>
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<tr>
<td>1993</td>
<td>3,100,000</td>
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<tr>
<td>1995</td>
<td>5,500,000</td>
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<tr>
<td>1997</td>
<td>7,500,000</td>
</tr>
<tr>
<td>1999</td>
<td>19,000,000</td>
</tr>
<tr>
<td>2000</td>
<td>28,100,000</td>
</tr>
</tbody>
</table>

Number of transistors per chip doubles every 18 to 24 months
MOSFET Layout and Cross-Section

Top View:

Cross Section:
N-channel MOSFET

**Schematic Cross-Sectional View**

- polysilicon gate
- source
drain
- SiO₂
- Al
- n⁺
- p⁺
- CVD oxide
- p-type substrate

**Layout (Top View)**

4 lithography steps are required:
1. active area
2. gate electrode
3. contact
4. metal interconnects
Computing the Output Capacitance

Example 5.4 (pp. 197-203)

\[ \text{In} \rightarrow \text{Out} \]

\[ \frac{W}{L} = \frac{9\lambda}{2\lambda} \]

\[ \frac{W}{L} = \frac{3\lambda}{2\lambda} \]

\[ 2\lambda = 0.25 \mu m \]

Metal1

Poly-Si

PMOS

\( W/L = 9\lambda/2\lambda \)

NMOS

\( W/L = 3\lambda/2\lambda \)

GND

V\(_{DD}\)
Integrated Circuit Fabrication

Goal:
Mass fabrication (i.e. simultaneous fabrication) of many “chips”, each a circuit (e.g. a microprocessor or memory chip) containing millions or billions of transistors

Method:
Lay down thin films of semiconductors, metals and insulators and pattern each layer with a process much like printing (lithography).

Materials used in a basic CMOS integrated circuit:
- Si substrate – selectively doped in various regions
- SiO$_2$ insulator
- Polycrystalline silicon – used for the gate electrodes
- Metal contacts and wiring
Si Substrates (Wafers)

Crystals are grown from a melt in boules (cylinders) with specified dopant concentrations. They are ground perfectly round and oriented (a “flat” or “notch” is ground along the boule) and then sliced like baloney into wafers. The wafers are then polished.

Typical wafer cost: $50
Sizes: 150 mm, 200 mm, 300 mm diameter

“notch” indicates crystal orientation
Adding Dopants into Si

Suppose we have a wafer of Si which is p-type and we want to change the surface to n-type. The way in which this is done is by ion implantation. Dopant ions are shot out of an “ion gun” called an ion implanter, into the surface of the wafer.

Typical implant energies are in the range 1-200 keV. After the ion implantation, the wafers are heated to a high temperature (~1000°C). This “annealing” step heals the damage and causes the implanted dopant atoms to move into substitutional lattice sites.
Dopant Diffusion

- The implanted depth-profile of dopant atoms is peaked.

- In order to achieve a more uniform dopant profile, high-temperature annealing is used to diffuse the dopants.

- Dopants can also be directly introduced into the surface of a wafer by diffusion (rather than by ion implantation) from a dopant-containing ambient or doped solid source.
The favored insulator is pure silicon dioxide ($\text{SiO}_2$).

A $\text{SiO}_2$ film can be formed by one of two methods:

1. Oxidation of Si at high temperature in $\text{O}_2$ or steam ambient
2. Deposition of a silicon dioxide film
Thermal Oxidation

\[ Si + O_2 \rightarrow SiO_2 \quad \text{or} \quad Si + 2H_2O \rightarrow SiO_2 + 2H_2 \]

“dry” oxidation \hspace{1cm} “wet” oxidation

- **Temperature range:**
  - 700°C to 1100°C

- **Process:**
  - \(O_2\) or \(H_2O\) diffuses through SiO\(_2\) and reacts with Si at the interface to form more SiO\(_2\)
  - 1 \(\mu m\) of SiO\(_2\) formed consumes \(\sim 0.5 \mu m\) of Si

\[ t \propto \sqrt{t} \quad t \propto \sqrt{t} \]

\[ \text{oxide thickness} \]

\[ \text{time, } t \]
Thermal oxidation grows SiO$_2$ on Si, but it consumes Si, so the wafer gets thinner. Suppose we grow 1 $\mu$m of oxide:

Silicon wafer, 100 $\mu$m thick

99 $\mu$m thick Si, with 1 $\mu$m SiO$_2$ all around
$\Rightarrow$ total thickness = 101 $\mu$m
The thermal oxidation rate slows with oxide thickness. Consider a Si wafer with a patterned oxide layer:

Now suppose we grow 0.1 μm of SiO₂:

Note the 0.04μm step in the Si surface!
Selective Oxidation Techniques

**Window Oxidation**

**Local Oxidation (LOCOS)**
Chemical Vapor Deposition (CVD) of SiO$_2$

$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$  

“LTO”

- **Temperature range:**
  - 350$^\circ$C to 450$^\circ$C for silane

- **Process:**
  - Precursor gases dissociate at the wafer surface to form SiO$_2$
  - No Si on the wafer surface is consumed

- **Film thickness is controlled by the deposition time**

\[ \text{oxide thickness} = \propto t \]
Polycrystalline silicon (“poly-Si”):

Like SiO$_2$, Si can be deposited by Chemical Vapor Deposition:
- Wafer is heated to $\sim 600^\circ$C
- Silicon-containing gas (SiH$_4$) is injected into the furnace:
$$\text{SiH}_4 = \text{Si} + 2\text{H}_2$$

Properties:
- sheet resistance (heavily doped, 0.5 $\mu$m thick) = 20 $\Omega/\square$
- can withstand high-temperature anneals $\rightarrow$ major advantage
Physical Vapor Deposition ("Sputtering")

Used to deposit Al films:

Highly energetic argon ions batter the surface of a metal target, knocking atoms loose, which then land on the surface of the wafer.

Sometimes the substrate is heated, to ~300°C

Gas pressure: 1 to 10 mTorr

Deposition rate $\propto I \cdot S$
Patterning the Layers

Planar processing consists of a sequence of **additive** and **subtractive** steps with **lateral patterning**

- **oxidation**
- **deposition**
- **etching**
- **lithography**

**Lithography** refers to the process of transferring a pattern to the surface of the wafer

**Equipment, materials, and processes needed:**

- A mask (for each layer to be patterned) with the desired pattern
- A light-sensitive material (called **photoresist**) covering the wafer so as to receive the pattern
- A light source and method of projecting the image of the mask onto the photoresist ("**printer**" or "**projection stepper**" or "**projection scanner**")
- A method of “developing” the photoresist, that is selectively removing it from the regions where it was exposed
The Photo-Lithographic Process

1. Oxidation
2. Optical mask
3. Photoresist coating
4. Spin, rinse, dry
5. Acid etch
6. Process step
7. Photoresist removal (ashing)
8. Photoresist exposure
9. Photoresist develop

The process involves applying a photoresist coating, then exposing it to light through a mask, followed by development and etching to create the desired pattern.
Photoresist Exposure

- A glass mask with a black/clear pattern is used to expose a wafer coated with \( \sim 1 \ \mu m \) thick photoresist.

Mask image is demagnified by \( nX \)
- “10X stepper”
- “4X stepper”
- “1X stepper”

Areas exposed to UV light are susceptible to chemical removal.
Exposure using “Stepper” Tool

- scribe line
- images
- wafer

field size increases with technology generation

Translational motion
Photoresist Development

• Solutions with high pH dissolve the areas which were exposed to UV light; unexposed areas are not dissolved.
Lithography Example

- Mask pattern (on glass plate)

- Look at cuts (cross sections) at various planes
  
  (A-A and B-B)
“A-A” Cross-Section

The resist is exposed in the ranges $0 < x < 2 \, \mu m$ & $3 < x < 5 \, \mu m$:

The resist will dissolve in high pH solutions wherever it was exposed:
“B-B” Cross-Section

The photoresist is exposed in the ranges $0 < x < 5 \, \mu m$:

- Mask pattern
- Resist
- Resist after development
In order to transfer the photoresist pattern to an underlying film, we need a “subtractive” process that removes the film, ideally with minimal change in the pattern and with minimal removal of the underlying material(s).

→ **Selective etch processes** (using plasma or aqueous chemistry) have been developed for most IC materials.

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**Pattern Transfer by Etching**

First: pattern photoresist

![Diagram of pattern transfer](image)

We have exposed mask pattern, and developed the resist.

Next: Etch oxide

![Diagram of etching oxide](image)

Etch stops on silicon (“selective etchant”) only resist is attacked.

Last: strip resist

![Diagram of resist stripping](image)

Only resist is attacked.

**Jargon for this entire sequence of process steps:** “pattern using XX mask”
Photolithography

- 2 types of photoresist:
  - positive tone: portion exposed to light will be dissolved in developer solution
  - negative tone: portion exposed to light will NOT be dissolved in developer solution

from Atlas of IC Technologies by W. Maly
Lithography trends

- Lithography determines the minimum feature size and limits the throughput that can be achieved in an IC manufacturing process. Thus, lithography research & development efforts are directed at:

1. achieving higher resolution
   - shorter wavelengths
     \[365 \text{ nm} \rightarrow 248 \text{ nm} \rightarrow 193 \text{ nm} \rightarrow 13 \text{ nm}\]
     - "i-line" "DUV" "EUV"

2. improving resist materials
   - higher sensitivity, for shorter exposure times
     (throughput target is 60 wafers/hr)
Plasmas are used to enhance various processes:

- **CVD**: Energy from RF electric field assists the dissociation of gaseous molecules, to allow for thin-film deposition at higher rates and/or lower temperatures.

- **Etch**: Ionized etchant species are more reactive and can be accelerated toward wafer (biased at negative DC potential), to provide directional etching for more precise transfer of lithographically defined features.

![Reactive Ion Etcher](image)
Dry Etching vs. Wet Etching

- Better etch selectivity
- Better control of etched feature sizes

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Dry Etching (Anisotropic)
- Reactive Ion Etching (DRIE)
  - Better control of etched feature sizes

Wet Etching (Isotropic)
- More uniform etching
  - Better etch selectivity

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From Atlas of IC Technologies by W. Maly
Micromachining to make MEMS devices

An example of a micromachined part – the world’s smallest guitar. The strings are only 5 nm wide and they actually can be made to vibrate when touched (carefully) with a fine probe. Guitar made by SURFACE MICROMACHING (below).

Surface Micromachining:

- Structures are formed on a sacrificial layer on a substrate and then the sacrificial layer is etched away (usually etching very little material, such as a glass doped for rapid etching).

- Easily etched layer (e.g., phosphorous doped glass, PSG)

- Pattern sacrificial layer (PSG)

- Deposit and pattern structural material (e.g., polysilicon)

- Etch away sacrificial layer

- Freestanding beam

Micromachining to make MEMS devices
Rapid Thermal Annealing (RTA)

Sub-micron MOSFETs need ultra-shallow junctions ($x_j<50$ nm)
→ Dopant diffusion during “activation” anneal must be minimized
→ Short annealing time (<1 min.) at high temperature is required

- Ordinary furnaces (e.g. used for thermal oxidation and CVD) heat and cool wafers at a slow rate (<50°C per minute)
- Special annealing tools have been developed to enable much faster temperature ramping, and precise control of annealing time
  - ramp rates as fast as 200°C/second
  - anneal times as short as 0.5 second
  - typically single-wafer process chamber:
Chemical Mechanical Polishing (CMP)

- **Chemical mechanical polishing** is used to planarize the surface of a wafer at various steps in the process of fabricating an integrated circuit.
  - interlevel dielectric (ILD) layers
  - shallow trench isolation (STI)
  - copper metallization
    - “damascene” process

Oxide Isolation of Transistors

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<table>
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<th>p+</th>
<th>n+</th>
<th>n+</th>
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<tr>
<td>n</td>
<td>SiO₂</td>
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<td>p</td>
</tr>
<tr>
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<td>p</td>
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IC with 5 layers of Al wiring
Copper Metallization

“Dual Damascene Process”
(IBM Corporation)

1. Oxide deposition

2. Stud lithography and reactive ion etch

3. Wire lithography and reactive ion etch

4. Stud and wire metal deposition

5. Metal chemical-mechanical polish

courtesy of Sung Gyu Pyo, Hynix Semiconductor
CMP Tool

- Wafer is polished using a slurry containing
  - silica particles (10-90nm particle size)
  - chemical etchants (e.g. HF)

- Backing film provides elasticity between carrier and wafer

- Polishing pad made of polyurethane, with 1 mm perforations
  - rough surface to hold slurry