Announcements

• You should now purchase the reader *EECS 42: Introduction to Electronics for Computer Science*, containing reference material from texts by Howe and Sodini and by Rabaey et al., at Copy Central at Hearst near Euclid Avenue.

• Midterm exam solutions with histogram of results available from Chris, 253 Cory, or from your GSI

OUTLINE

– Propagation delay
– Energy consumption of simple RC circuit
– Examples of RC-circuit transient response

Reading

Start reading Howe & Sodini Ch. 2.1-2.4.1
Voltage Ranges for Digital Signals

• A digital signal varies with time, typically between ground (0 Volts) and the power supply voltage ($V_{supply}$).

• A digital voltage signal has two defined states “high” (corresponding to logical state 1) or “low” (corresponding to logical state 0)

• Each of the two states corresponds to a range of voltages, for example:

  logical 1 state: $voltage > \frac{V_{supply}}{2}$
  logical 0 state: $voltage < \frac{V_{supply}}{2}$
Logic Gates and What’s Inside

Figure 0.1 CMOS circuits and their schematic symbols
Propagation Delay $t_p$

- The propagation delay $t_p$ of a logic gate defines how quickly the output voltage responds to a change in input voltage. It is measured between the 50% transition points of the input and output voltage waveforms.

Example: Output voltage changing from “low” to “high”

$$V_{out}(t) = V_{supply} \left(1 - e^{-t/R_p C}\right)$$

![Diagram showing voltage waveforms with time and voltage axes]
**Formula for Propagation Delay $t_p$**

- A logic gate can display different response times for rising and falling input waveforms, so two definitions of propagation delay are necessary.

\[
t_p = \frac{t_{pLH} + t_{pHL}}{2}
\]

**Example:** Output voltage changing from “high” to “low”

\[
V_{out}(t) = V_{\text{high}}e^{-t/R_NC}
\]
Energy Consumption of Simple RC Circuit

- In charging a capacitor, the energy that is delivered to the capacitor is \( \frac{1}{2} CV_{\text{supply}}^2 \)

- The energy delivered by the source is

\[
W = \int_{0}^{\infty} p(t) \, dt = \int_{0}^{\infty} v(t) i(t) \, dt = \int_{0}^{\infty} V_{\text{supply}} \left( C \frac{dv}{dt} \right) \, dt = CV_{\text{supply}}^2
\]

How much energy is delivered to the resistor \( R_P \)?
• In discharging a capacitor, the energy that is delivered to the resistor $R_N$ is $\frac{1}{2} CV_{\text{supply}}^2$.

• Thus, in one complete cycle (charging and discharging), the total energy delivered by the voltage source is $CV_{\text{supply}}^2$. 
Power-Delay Product

- The propagation delay and power consumption of a digital logic gate are related:
  - The smaller the propagation delay, the higher the \textit{switching frequency} $f$ can be.
  - $\rightarrow$ higher dynamic power consumption

\[
  P_{\text{dynamic}} \propto fCV^2_{\text{supply}}
\]

- For a given digital-IC technology, the product of power consumption and propagation delay (the “power-delay product”) is generally a constant.
  - PDP is simply the energy consumed by the logic gate per switching event, and is a quality measure.
The switch is closed for $t < 0$, and then opened at $t = 0$. Find the voltage $v_c(t)$ for $t \geq 0$.

1. Determine the initial voltage $v_c(0)$
2. Determine the final voltage $v_c(\infty)$

3. Calculate the time constant $\tau$
\[
v_c(t) = v_c(\infty) + [v_c(0) - v_c(\infty)] e^{-t/\tau}
\]
Random-access memory (RAM): array of thousands of memory elements (cells) that store computer instructions and data. Any cell can be accessed in a single operational cycle.

The simpler and thus denser random-access memory, dynamic random-access memory or DRAM, uses a single transistor and a capacitor to form the memory cell (see next slide). The transistor acts as a switch to connect the capacitor to the column, or bit line when the row, or word line has a high voltage on it. The capacitor stores charge to indicate a 1. When the switches for a row are closed, the charge on a capacitor that is storing a 1 will cause a voltage rise on the corresponding column wire. A sense amplifier on each column amplifies the small voltage change back to digital levels.

Each cell must be refreshed frequently because (a) the reading action diminishes the charges stored on the capacitors, as does (b) leakage in the capacitors.
Dynamic Random-Access Memory (DRAM)
DRAM (Dynamic Memory Device) Example

- The operation of a DRAM cell (which stores one bit of information) can be modeled as an RC circuit:

\[ V_{\text{bit-line}} - V_{\text{cell}} + V_{\text{bit-line}} \]

\[ C_{\text{cell}} = 0.1 \text{pF} \]

\[ R = 10 \text{k}\Omega \]

\[ C_{\text{bit-line}} = 1 \text{pF} \]

- Suppose the bit line is pre-charged to 1 V before the cell is read, and that the cell is programmed to 2 V. What is the final value of the bit-line voltage, after the switch is closed?
DRAM Example (cont’d)

• The charges stored on $C_{cell}$ and $C_{bit-line}$ prior to reading are

\[ Q_{cell,initial} = C_{cell} V_{cell,initial} = \left(10^{-13} \text{ F}\right) \left(2 \text{ V}\right) = 2 \times 10^{-13} \text{ C} \]

and

\[ Q_{bit-line,initial} = C_{bit-line} V_{bit-line,initial} = \left(10^{-12} \text{ F}\right) \left(1 \text{ V}\right) = 1 \times 10^{-12} \text{ C} \]

\[ Q_{total,initial} = Q_{cell,initial} + Q_{bit-line,initial} = 1.2 \times 10^{-12} \text{ C} \]

• The final voltages on each capacitor are equal.

\[ \Rightarrow Q_{total,final} = C_{cell} V_{final} + C_{bit-line} V_{final} \]

• Total charge is conserved:

\[ Q_{total,final} = \left(C_{cell} + C_{bit-line}\right) V_{final} = Q_{total,initial} \]

\[ V_{final} = \frac{Q_{total,initial}}{C_{cell} + C_{bit-line}} = \frac{1.2 \times 10^{-12} \text{ C}}{1.1 \times 10^{-12} \text{ F}} \approx 1.09 \text{ Volts} \]
DRAM Example (cont’d)

- Sketch the bit-line voltage waveform

\[ V_{\text{bit-line}} (V) \]

- Is energy conserved? Explain.
Plan

• We will be studying semiconductor devices and technology for the next several weeks
  – How does a transistor work?
    (need to learn about semiconductors and diode devices first)
  – How are transistors used as amplifiers?
    • modeled as dependent current source
  – How are transistors used to implement digital logic gates?
    • modeled as resistive switch
    (circuit performance is limited by RC delay)