Week 9a

OUTLINE

• MOSFET $I_D$ vs. $V_{GS}$ characteristic
• Circuit models for the MOSFET
  – resistive switch model
  – small-signal model

Reading

• Rabaey et al.: Chapter 3.3.2
• Hambley: Chapter 12 (through 12.5); Section 10.8
  (Linear Small-Signal Equivalent Circuits)
**$I_D$ vs. $V_{DS}$ Characteristics**

The MOSFET $I_D$-$V_{DS}$ curve consists of two regions:

1) **Resistive or “Triode” Region:** $0 < V_{DS} < V_{GS} - V_T$

   \[
   I_D = k'_n \frac{W}{L} \left[ V_{GS} - V_T - \frac{V_{DS}}{2} \right] V_{DS}
   \]

   where $k'_n = \mu_n C_{ox}$

2) **Saturation Region:** $V_{DS} > V_{GS} - V_T$

   \[
   I_{DSAT} = \frac{k'_n}{2} \frac{W}{L} \left( V_{GS} - V_T \right)^2
   \]

   where $k'_n = \mu_n C_{ox}$

   **“CUTOFF” region:** $V_G < V_T$
Overview of NMOSFET Regions

1. Cutoff region:
   Conditions: \( V_{GS} < V_T \), any value of \( V_{DS} \)
   \[ I_D = 0 \]

2. Linear (or Resistive, or Triode) region:
   \( V_{GS} > V_T, (V_{GS} - V_T) > V_{DS} \)
   \[ I_D = (f_1 \times f_2 \times f_3) V_{DS} \]
   where
   \( f_1 = \mu C_{ox} \) (depends on the fabrication process)
   \( f_2 = W/L \) (chosen by the design engineer)
   \( f_3 = f_3(V_{GS}, V_T, V_{DS}) = [V_{GS} - V_T - V_{DS}/2] \)
   \( \sim (V_{GS} - V_T) \) if \( (V_{GS} - V_T) >> V_{DS}/2 \)

3. Saturation region:
   \( V_{DS} > (V_{GS} - V_T) = V_{DSaturation} = (V_{GS} - V_T)^2 \)
   \[ I_D = (1/2) f_1 \times f_2 \times (V_{GS} - V_T)^2 \]

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Week 9a, Slide 3
Prof. White
MOSFET $I_D$ vs. $V_{GS}$ Characteristic

- Typically, $V_{DS}$ is fixed when $I_D$ is plotted as a function of $V_{GS}$.

**Long-channel MOSFET**

$V_{DS} = 2.5 \, \text{V} > V_{DSAT}$

**Short-channel MOSFET**

$V_{DS} = 2.5 \, \text{V} > V_{DSAT}$
MOSFET $V_T$ Measurement

- $V_T$ can be determined by plotting $I_D$ vs. $V_{GS}$, using a low value of $V_{DS}$:

$$I_D = k'_n \frac{W}{L} \left[ V_{GS} - V_T - \frac{V_{DS}}{2} \right] V_{DS}$$
Subthreshold Conduction (Leakage Current)

- The transition from the ON state to the OFF state is gradual. This can be seen more clearly when $I_D$ is plotted on a logarithmic scale:

- In the subthreshold ($V_{GS} < V_T$) region,

  $$I_D \propto \exp \left( \frac{q V_{GS}}{n k T} \right)$$

  This is essentially the channel-source pn junction current. (n, the emission factor, is between 1 and 2) (Some electrons diffuse from the source into the channel, if this pn junction is forward biased.)
Qualitative Explanation for Subthreshold Leakage

- The channel \( V_c \) (at the Si surface) is capacitively coupled to the gate voltage \( V_G \):

Using the capacitive voltage divider formula:

\[
\Delta V_c = \frac{C_{ox}}{C_{ox} + C_{dep}} \Delta V_G
\]

The forward bias on the channel-source pn junction increases with \( V_G \) scaled by the factor \( C_{ox} / (C_{ox} + C_{dep}) \)

\[
\Rightarrow n = \frac{C_{ox} + C_{dep}}{C_{ox}} = 1 + \frac{C_{dep}}{C_{ox}}
\]
Slope Factor (or Subthreshold Swing) $S$

- $S$ is defined to be the inverse slope of the log ($I_D$) vs. $V_{GS}$ characteristic in the subthreshold region:

$$1/S = \frac{q}{kT} \ln(10)$$

**Units:** Volts per decade

Note that $S \geq 60$ mV/dec at room temperature:

$$\left(\frac{kT}{q}\right) \ln(10) = 60 \text{ mV}$$
**$V_T$ Design Trade-Off**

(Important consideration for digital-circuit applications)

- Low $V_T$ is desirable for high ON current
  \[ I_{DSAT} \propto (V_{DD} - V_T)^\eta \quad 1 < \eta < 2 \]
  where $V_{DD}$ is the power-supply voltage

...but high $V_T$ is needed for low OFF current

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![Graph showing the trade-off between $V_T$ and $I_{DS}$](Image)
The MOSFET as a Resistive Switch

- For digital circuit applications, the MOSFET is either OFF \((V_{GS} < V_T)\) or ON \((V_{GS} = V_{DD})\). Thus, we only need to consider two \(I_D\) vs. \(V_{DS}\) curves:
  1. the curve for \(V_{GS} < V_T\)
  2. the curve for \(V_{GS} = V_{DD}\)
Equivalent Resistance $R_{eq}$

- In a digital circuit, an n-channel MOSFET in the ON state is typically used to discharge a capacitor connected to its drain terminal:
  - gate voltage $V_G = V_{DD}$
  - source voltage $V_S = 0$ V
  - drain voltage $V_D$ initially at $V_{DD}$, discharging toward 0 V

The value of $R_{eq}$ should be set to the value which gives the correct propagation delay (time required for output to fall to $\frac{1}{2}V_{DD}$):

\[
R_{eq} \approx \frac{3}{4} \frac{V_{DD}}{I_{DSATn}} \left(1 - \frac{5}{6} \lambda_n V_{DD} \right)
\]
Figure 0.1 CMOS circuits and their schematic symbols
Typical MOSFET Parameter Values

- For a given MOSFET fabrication process technology, the following parameters are known:
  - $V_T$ (~0.5 V)
  - $C_{ox}$ and $k'$ (<0.001 A/V²)
  - $V_{DSAT}$ (≤ 1 V)
  - $\lambda$ (≤ 0.1 V⁻¹)

Example $R_{eq}$ values for 0.25 µm technology ($W = L$):

<table>
<thead>
<tr>
<th>$V_{DD}$ (V)</th>
<th>1</th>
<th>1.5</th>
<th>2</th>
<th>2.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS (kΩ)</td>
<td>35</td>
<td>19</td>
<td>15</td>
<td>13</td>
</tr>
<tr>
<td>PMOS (kΩ)</td>
<td>115</td>
<td>55</td>
<td>38</td>
<td>31</td>
</tr>
</tbody>
</table>

How can $R_{eq}$ be decreased?
P-Channel MOSFET Example

- In a digital circuit, a p-channel MOSFET in the ON state is typically used to charge a capacitor connected to its drain terminal:
  - gate voltage $V_G = 0 \text{ V}$
  - source voltage $V_s = V_{DD}$ (power-supply voltage)
  - drain voltage $V_D$ initially at 0 V, charging toward $V_{DD}$

\[ R_{eq} \approx \frac{3}{4} \left| I_{DSATp} \right| \left( 1 - \frac{5}{6} \lambda_p V_{DD} \right) \]

\[ I_{DSAT} = -\frac{k_p}{2} \frac{W}{L} (V_{DD} - |V_{Tp}|)^2 \]
Common-Source (CS) Amplifier

- The input voltage $v_s$ causes $v_{GS}$ to vary with time, which in turn causes $i_D$ to vary.

- The changing voltage drop across $R_D$ causes an amplified (and inverted) version of the input signal to appear at the drain terminal.

$$V_{DD} - v_{OUT} = v_{DS} \quad \text{(KVL)}$$

$$v_{IN} = v_{GS}$$

$$v_{OUT} = v_{DS}$$

$$v_{DS} = -i_D R_D$$
Notation

- Subscript convention:
  - $V_{DS} \equiv V_D - V_S$, $V_{GS} \equiv V_G - V_S$, etc.

- Double-subscripts denote DC sources:
  - $V_{DD}$, $V_{CC}$, $I_{SS}$, etc.

- To distinguish between DC and incremental components of an electrical quantity, the following convention is used:
  - **DC quantity**: upper-case letter with upper-case subscript
    - $I_D$, $V_{DS}$, etc.
  - **Incremental quantity**: lower-case letter with lower-case subscript
    - $i_d$, $v_{ds}$, etc.
  - **Total (DC + incremental) quantity**:
    - lower-case letter with upper-case subscript
      - $i_D$, $v_{DS}$, etc.
Load-Line Analysis of CS Amplifier

- The operating point of the circuit can be determined by finding the intersection of the appropriate MOSFET $i_D$ vs. $v_{DS}$ characteristic and the load line:

$$V_{DD} = R_D i_D + v_{DS}$$

**load-line equation:**

- $R_D = 10k\Omega$
- $I_D (V_{DS}=0) = \frac{V_{DD}}{10k\Omega} = \frac{5}{10^4}$

**Δ $v_{GS}$ = +0.5V**

**Δ $v_{DS}$ = -1.5V**

$v_{DS} (V)$

$i_D (mA)$

$v_{GS} (V)$

Load Line

$v_{DD} / R_D$
Voltage Transfer Function

Goal:
Operate the amplifier in the high-gain region, so that small changes in $v_{IN}$ result in large changes in $v_{OUT}$

(1): transistor biased in cutoff region
(2): $v_{IN} > V_T$; transistor biased in saturation region
(3): transistor biased in saturation region
(4): transistor biased in “resistive” or “triode” region
Quiescent Operating Point

• The operating point of the amplifier for zero input signal \( v_s = 0 \) is often referred to as the **quiescent operating point**. (Another word: *bias*.)
  
  – The bias point should be chosen so that the output voltage is approximately centered between \( V_{DD} \) and 0 V.
  
  – \( v_s \) varies the input voltage around the input bias point.

**Note:** The relationship between \( v_{OUT} \) and \( v_{IN} \) is not linear; this can result in a distorted output voltage signal. If the input signal amplitude is very small, however, we can have amplification with negligible distortion.
Bias Circuit Example
Rules for Small-Signal Analysis

• A DC supply \textit{voltage source} acts as a \textit{short circuit}  
  – Even if AC current flows through the DC voltage source, 
    the AC voltage across it is zero.

• A DC supply \textit{current source} acts as an \textit{open circuit}  
  – Even if AC voltage is applied across the current source, 
    the AC current through it is zero.
NMOSFET Small-Signal Model

\[ i_d = \frac{\partial i_D}{\partial v_{GS}} v_{gs} + \frac{\partial i_D}{\partial v_{DS}} v_{ds} = g_m v_{gs} + g_o v_{ds} \]

\[ g_m \equiv \frac{\partial i_D}{\partial v_{GS}} \approx \frac{W}{L} k'(V_{GS} - V_T) \quad \text{transconductance} \]

\[ g_o \equiv \frac{\partial i_D}{\partial v_{DS}} \approx \lambda I_D \quad \text{output conductance} \]
If $L$ is small, the effect of $\Delta L$ to reduce the inversion-layer "resistor" length is significant

$\rightarrow I_D$ increases noticeably with $\Delta L$ (i.e. with $V_{DS}$)

$$I_D = I_D'(1 + \lambda V_{DS})$$

$\lambda$ is the slope

$I_D'$ is the intercept

Channel-Length Modulation
Small-Signal Equivalent Circuit

\[ v_{out} = -g_m v_{gs} \left( r_o \parallel R_D \right) \]

voltage gain \[ A_v = \frac{v_{out}}{v_{in}} = -g_m \left( r_o \parallel R_D \right) \]