1)

\[ t_{p_a} = \ln(2) \cdot 3R \cdot C_L = 3 \cdot \ln(2) \cdot RC_L \]
\[ t_{p_b} = \ln(2) \cdot \frac{3R}{2} \cdot C_L = 1.5 \cdot \ln(2) \cdot RC_L \]
\[ t_{p_c} = \ln(2) \cdot \frac{3R}{3} \cdot C_L = \ln(2) \cdot RC_L \]

2)

\[ t_1 = t_0 + t_{p_a} \]
\[ t_2 = t_0 + t_{p_b} \]
\[ t_3 = t_0 + t_{p_c} \]
2) \[ f = B \cdot C \]
\[ f = \overline{B} + \overline{C} \]
2) Yes, it is equivalent. It uses less transistors and utilizes smaller transistors, reducing the input capacitances.

3) It is a static CMOS gate. It does not have complementary PUI/PID networks, but the two networks operate as if they are complementary. This property (that only some logical functions have) is called "self-duality."
For PLOS weaker than NMOS (2/1)

\[ TLE = \frac{4}{3} \times \frac{5}{3} \times \frac{5}{3} \times \frac{5}{3} \]

\[ B = 4 \]

\[ F = 200 \]

\[ PE = 6914 \implies EF = \sqrt[3]{PE} \approx 3.54 \]

\[ f = \frac{\text{CL}}{EF} \approx 56.5 \]

\[ e = \frac{f}{EF} \cdot LE_e \approx 37.2 \]

\[ d = \frac{e}{EF} \cdot LE_d \approx 17.92 \]

\[ c = \frac{d}{EF} \approx 4.95 \]

\[ b = B_b \cdot \frac{c}{EF} \cdot LE_b \approx 9.38 \]

\[ a = \frac{b}{EF} \cdot LE_a \approx 3.52 \]

The fact that \( a \) is not exactly 3.52 is due to rounding errors.
For PMOS equal to NMOS

\[ TLE = \frac{3}{2} \cdot \frac{3}{2} \cdot 2.2 = 9 \]

\[ B = 4 \]
\[ F = 200 \]
\[ P_E = 7200 \Rightarrow EF = \sqrt[3]{PE} \approx 3.56 \]

\[ f = \frac{C_L}{EF} \approx 56 \]
\[ e = \frac{f}{EF} \cdot LE_e = 31.46 \]
\[ d = \frac{e}{EF} \cdot LE_d = 17.67 \]
\[ c = \frac{d}{EF} = 4.96 \]
\[ b = B_e \cdot \frac{c}{EF} \cdot LE_b = 8.36 \]
\[ a = \frac{b}{EF} \cdot LE_a = 3.52 \]

The fact that \( a \) is not exactly 3.52 is due to rounding errors.