Problem 1: Buffer Chain

Assume that we have the situation shown below with an inverter chain used to drive a large capacitive load \( F = 1000 \) with minimal delay. How many buffers (inverter stages) would be optimal (or near optimal) in this case? What should be the fanout, \( f \), be at each stage?

![Buffer Chain Diagram]

Problem 2: Transition Activity

Consider a 3-input NAND gate constructed from 2-input AND and NAND gates, as shown below. Assume that \( C_2 = C_1 = C \) and that there are no other capacitances in the circuit. The circuit is driven by supply \( V_{DD} \) and frequency \( f \). Each input has a probability of being high denoted \( P_X \) where \( X \) is G, H, I for the corresponding inputs.

![NAND Gate Diagram]

a) Calculate the total power dissipation in terms of \( V_{DD} \), \( f \), \( P_G \), \( P_H \), \( P_I \), and \( C \).

b) What is the total power dissipation (in \( \mu W \)) of the circuit for \( P_G = 0.7 \), \( P_H = 0.2 \), \( P_I = 0.5 \)? Assume that \( V_{DD} = 1 \), \( f = 1GHz \), and \( C = 10pF \).

c) For the same probabilities as part (b), suggest a more energy-efficient way of organizing the inputs. What is the power dissipation in this case?

Problem 3: Elmore Delay

For the following problem, \( C_G = C_D = 2fF/\mu m \), the minimum sized (1x) inverter has \( L = 0.1\mu m \), \( W_p = 1\mu m \), \( W_n = 1\mu m \) and for this technology \( R_{n,on} = R_{p,on} = 10k\Omega/\square \) (i.e. the on resistance of
a transistor with width $W$ and length $L$ is equal to $10k\Omega \frac{L}{W}$. Note that a 4x inverter has 4 times the width of a 1x inverter.

The wire has resistance $R_{\text{wire}} = 0.1\Omega/\square$, parallel plate capacitance $C_{\text{pp}} = 20\text{aF}/\mu\text{m}^2$ and the fringing capacitance per side of the wire is $C_{\text{fr}} = 14\text{aF}/\mu\text{m}$. The wire widths and lengths are shown in the diagram.

![Diagram of a transistor and wire model](image)

a) Using the $\pi$ wire model, draw the equivalent RC model. What is the propagation delay from a step at $V_{\text{in}}$ to $V_a$, $V_b$, and $V_c$.

b) What is the skew between pairs of $V_a$, $V_b$, and $V_c$? (i.e. what is the difference in arrival time between $V_a$ and $V_b$, $V_a$ and $V_c$, $V_b$ and $V_c$?)

**Problem 4: Arithmetic**

![Schematic of an arithmetic circuit](image)

a) Explain the functionality of the circuit shown above. (FA stands for full-adder, HA stands for half-adder)

b) What is the critical path of the circuit? You may assume that each of the FA, HA and XOR blocks have a delay equal to $t_{\text{gate}}$. Show the critical path on the schematic.

c) Design a circuit with exactly the same functionality but shorter critical path. You are allowed to use FA, HA and XOR blocks.