Midterm Exam

Name: ____________________________________________

ID number: ____________________________________________

Class (EECS151 or EECS251A): __________________________

This is a closed-book exam, but you are allowed a single sheet of notes. No calculators, phones, pads, or laptops. Each question is marked with its number of points (one point per expected minute of time), in the form “[EECS151 points / EECS251A points]” Start by answering the easier questions then move on to the more difficult ones. You can tear off the spare pages at the end of the booklet and/or use the backs of the pages to work out your answers. Neatly copy your answer to the allocated places. Neatness counts. We will deduct points if we need to work hard to understand your answer.

For all relevant problems, assume the following transistor switch model:

```
\[ W_n \quad G \quad \gamma \quad W_n C_G \]
```

Put your name and SID on each page.

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1. [10pts/14pts] Combinational Logic Design.

Consider the design of the combinational logic block that takes as input a 3-bit two's-complement integer, \( X \), and produces as output another 3-bit two's-complement integer representing the \textit{absolute value of} \( X \). Assume that the input integer is in the range of \(-3 \leq X \leq 3\).

(a) [4pts] In the space below draw the truth-table that represents the values of the output signals, \( y_2 \) (the most significant bit), \( y_1 \), and \( y_0 \) (the least significant bit) as a function of the inputs \( x_2, x_1, x_0 \). Beneath your truth table, write the sum-of-products canonical form for the output signals.

| \( x_2 \) \( x_1 \) \( x_0 \) | \( y_2 \) \( y_1 \) \( y_0 \) |
|---|---|---|
| 000 | 000 |  |
| 001 | 001 |  |
| 010 | 010 |  |
| 011 | 011 |  |
| 100 | - - - |  |
| 101 | 011 |  |
| 110 | 010 |  |
| 111 | 001 |  |

\( y_0 = x_2'x_1'x_0 + x_2'x_1x_0 + x_2x_1'x_0 + x_2x_1x_0 \)
\( y_1 = x_2'x_1x_0' + x_2'x_1x_0 + x_2x_1'x_0 + x_2x_1x_0' \)
\( y_2 = 0 \)

(b) [6pts] In the space below use K-maps to derive minimized sum-of-product forms for the output signals.

\( y_1 = x_2'x_1 + x_1x_0' + x_2x_1' \)
\( y_0 = x_0 \)

(c) [4pts] \textbf{For 251A students only}: Starting from the canonical forms use algebraic manipulation to find the optimized logic equations.
\[ y_0 = \bar{x}_2 \bar{x}_1 x_0 + \bar{x}_2 x_1 x_0 + x_2 \bar{x}_1 x_0 + x_2 x_1 x_0 \\
= \bar{x}_2 x_0 (\bar{x}_1 + x_1) + x_2 x_0 (\bar{x}_1 + x_1) \\
= \bar{x}_2 x_0 + x_2 x_0 \\
= x_0 (\bar{x}_2 + x_2) \\
= x_0 \]

For \( y_1 \) we can assume that \( x_2 \bar{x}_1 \bar{x}_0 = 1 \) because it is a “don’t care”.

\[ y_1 = \bar{x}_2 \bar{x}_1 \bar{x}_0 + \bar{x}_2 x_1 x_0 + x_2 \bar{x}_1 x_0 + x_2 x_1 \bar{x}_0 \\
= \bar{x}_2 \bar{x}_1 \bar{x}_0 + \bar{x}_2 x_1 x_0 + x_2 \bar{x}_1 x_0 + x_2 x_1 \bar{x}_0 + (\bar{x}_2 x_1 \bar{x}_0 + x_2 \bar{x}_1 \bar{x}_0) \\
= \bar{x}_2 x_1 \bar{x}_0 + x_2 x_1 x_0 + x_2 x_1 \bar{x}_0 + x_2 \bar{x}_1 x_0 + x_2 \bar{x}_1 \bar{x}_0 + x_2 x_1 \bar{x}_0 \\
= \bar{x}_2 x_1 (\bar{x}_0 + x_0) + (\bar{x}_2 + x_2) x_1 \bar{x}_0 + x_2 \bar{x}_1 (x_0 + \bar{x}_0) \\
= \bar{x}_2 x_1 + x_1 \bar{x}_0 + x_2 \bar{x}_1 \]
2. [7pts/7pts] Logic Gates.

For the combinational logic function:

\[ y = (\overline{x_7} + \overline{x_6} + \overline{x_5} + \overline{x_4})(\overline{x_3} + \overline{x_2} + \overline{x_1} + \overline{x_0}), \]

draw a minimal gate-level diagram for \( y \) as a function of \( x_7, x_6, x_5, x_4, x_3, x_2, x_1, \) and \( x_0 \) using only inverters and 2-input NANDs and NORs.

\[
\begin{align*}
y &= (\overline{x_7} + \overline{x_6} + \overline{x_5} + \overline{x_4})(\overline{x_3} + \overline{x_2} + \overline{x_1} + \overline{x_0}) \\
   &= (\overline{x_7}x_6 + \overline{x_5}x_4)(\overline{x_3}x_2 + \overline{x_1}x_0) \\
   &= (\overline{x_7}x_6 + \overline{x_5}x_4)(\overline{x_3}x_2 + \overline{x_1}x_0) \\
   &= \overline{x_7}x_6 + \overline{x_5}x_4 + \overline{x_3}x_2 + \overline{x_1}x_0 \\
   &= ((x_7 \text{ nand } x_6) \text{ nor } (x_5 \text{ nand } x_4)) \text{ nor } ((x_3 \text{ nand } x_2) \text{ nor } (x_1 \text{ nand } x_0))
\end{align*}
\]

![Diagram of gate-level circuit for y as a function of x7, x6, x5, x4, x3, x2, x1, and x0 using only inverters and 2-input NANDs and NORs.]
3. [8pts/12pts] FSMs.

Below is the Verilog description of a bit-serial adder. The circuit adds 2 integers, \( A \) and \( B \), generating one bit of the sum per clock cycle by taking one bit from each of the integers (least significant bit first). An add operation concludes when the rst signal is asserted on the same clock cycle as the most significant bit of the inputs.

```verilog
module BSAdd (clk, rst, a, b, s);
  input clk, rst,
  input a, b;
  output s;

  reg s, c;
  wire nc, ns;

  always @(posedge clk)
    begin
      s <= ns;
      if (rst) c <= 1b'0; else c <= nc;
    end

  assign {nc, ns} = a + b + c;

endmodule
```

In the space below draw the state-transistion-diagram for a finite state machine that matches the behavior of the above circuit.
[4pts] For 251A students only: Draw the circuit diagram matching the Verilog description using flip-flops and simple logic gates.
4. [6pts/10pts] CMOS logic.

Draw the single, complex gate, transistor level CMOS representation of the following functions. Size the transistors in each stage for equal worst-case pull-up and pull-down strength (i.e. \( R_{eq,pu} = R_{eq,pd} \)) to be the same as those of the reference inverter with equal pull-down and pull-up strength (\( W_p = 2W_n \)). Label the sizes in units of \( W_n \) on each schematic.

(a) [3pts] \( F_1 = (\overline{AB} + C) \).

(b) [3pts] \( F_2 = \overline{A} + \overline{B}\overline{C} \).
(c) [4pts] **For 251A students only:** Which 2-input Boolean logic function does the circuit below represent? Make sure to simplify the Boolean expression to the Boolean function you can recognize.
5. [9pts/9pts] Gate Sizing and Logical Effort.

Calculate the Logical Effort (LE) for each input (worst-case pull-down and pull-up path - e.g. \( LE_{A,pup} \), \( LE_{A,pdn} \)) of the gates below. Assume that in this technology PMOS has twice worse mobility than NMOS (i.e. for \( W_p = W_n \), \( R_p = 2R_n \)).

(a) [4pts]

(b) [5pts]

The technology has the following parameters: $V_{th,N} = 0.2 V$ and $|V_{th,P}| = 0.3 V$, $R_n = 2k \Omega \mu m$, $R_p = 3k \Omega \mu m$ at $V_{dd} = 1V$. Draw the voltage transfer characteristic ($V_{out}$ vs $V_A$) of the gates below with $W_p = W_n = 1 \mu m$.

(a) [4pts] Draw the VTC and determine $V_{OL}$, $V_{IL}$, $V_{OH}$, $V_{IH}$ and noise margins $NM_H$ and $NM_L$.

(b) [3pts]
(c) [4pts] For 251A students only: Assume that $V_A = V_{dd} - V_A$. 

(a) [4pts] Calculate the optimal number of inserted inverter stages and the delay normalized to the intrinsic inverter delay $t_{\text{p0}}$ for the following problem (assume $\gamma = 1$):

\[
\begin{array}{c}
C_{\text{in}} \quad \cdots \quad C_L = 64C_{\text{in}} \\
\end{array}
\]

(b) [6pts] In the circuit below calculate the optimal size of the middle inverter ($x$) for minimum total delay:

\[
\begin{array}{c}
C_{\text{in}} \\
\downarrow \\
xC_{\text{in}} \\
\downarrow \\
16C_{\text{in}} \\
\downarrow \\
C_L = 64C_{\text{in}} \\
\end{array}
\]

\[
\begin{array}{c}
C_w = 48C_{\text{in}} \\
\downarrow \\
C_L = 64C_{\text{in}} \\
\end{array}
\]
8. [10pts/15pts] Sizing the Logic Path.

For the circuit drawn below determine:

(a) [2pts] Mark the critical path in the circuit.
(b) [3pts] Calculate the path logical effort for the critical path in this circuit.

(c) [5pts] Size the gates for minimum delay ignoring wires and mark the value of the input capacitance of each gate. The first gate in the critical path has input capacitance $C_{in}$, and the load capacitance at the output is $C_L = \frac{125}{3}C_{in}$. 
(d) [5pts] **For 251A students only:** Using the sizes from your previous answer, a wire capacitance of $C_{wire} = \frac{5}{2}C_{in}$ is inserted between each gate. Assuming $\gamma = 1$, calculate the delay through the critical path normalized to the intrinsic inverter delay $t_{\mu 0}$?
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