Logical Effort
Question #1

How to best combine logic and drive for a big capacitive load?
Question #2

- All of these are “decoders”
  - Which one is “best”?
Method to answer both of these questions

- Extension of buffer sizing problem
- Logical effort
Complex Gate Sizing
Complex Gate Sizing: NAND-2 Example

\[ C_{\text{gnand}} = 4C_G = (4/3) \ C_{\text{ginv}} \]

\[ C_{\text{dnand}} = 6C_D = 6\gamma C_G = 2\gamma C_{\text{ginv}} \]

\[ f = C_L/C_{\text{gnand}} = (3/4) \ C_L/C_{\text{ginv}} \]

\[ t_{\text{pNAND}} = kR_N(C_{\text{dnand}} + C_L) \]

\[ = kR_N(2\gamma C_{\text{ginv}} + C_L) \]

\[ = kR_N C_{\text{ginv}} (2\gamma + C_L/C_{\text{ginv}}) \]

\[ = t_{\text{inv}} (2\gamma + (4/3)f) \]
Logical Effort

- Defines ease of gate to drive external capacitance
- Inverter has the smallest logical effort and intrinsic delay of all static CMOS gates
- Logical effort LE is defined as:
  - \( \frac{R_{eq,\text{gate}}C_{in,\text{gate}}}{R_{eq,\text{inv}}C_{in,\text{inv}}} \)
  - Easiest way to calculate (usually):
    - Size gate to deliver same current as an inverter, take ratio of gate input capacitance to inverter capacitance
- LE increases with gate complexity
Logical Effort

\[ t_{pgate} = t_{inv} (p + LEf) \]

Measure everything in units of \( t_{inv} \) (divide by \( t_{inv} \)):

- \( p \) – intrinsic delay - gate parameter ≠ \( f(W) \)
- \( LE \) – logical effort – gate parameter ≠ \( f(W) \)
- \( f \) – electrical fanout = \( C_L/C_{in} \) = \( f(W) \)

Normalize everything to an inverter:
- \( LE_{inv} = 1 \), \( p_{inv} = \gamma \)
Delay of a Logic Gate

Gate delay:

\[ Delay = EF + p \]  
(measured in units of \( t_{inv} \))

- effective fanout
- intrinsic delay

Effective fanout:

\[ EF = LE f \]

- logical effort
- electrical fanout \( = C_L/C_{in} \)

Logical effort is a function of topology, independent of sizing
Effective fanout is a function of load/gate size
Logical Effort of Gates

$p = \gamma \cdot \text{Fan-in} \quad \text{(for top input)}$

Graph showing the relationship between normalized delay ($d$) and fan-out ($f$) for different logical effort ($LE$) and normalized delays ($t_{pNAND-2}$ and $t_{pINV}$).

$LE = \gamma \cdot \text{Fan-in}$
Delay Of NOR-2 Gate

1. Size for same resistance as inverter
2. LE = ratio of input cap of gate versus inverter

Intrinsic capacitance \( C_{\text{dnor}} \) = 
\[ t_{\text{pint}} \text{ (NOR)} = \]
Any logic function can be implemented using NOR gates only or NAND gates only!

Which of the two approaches is preferable in CMOS (from a performance perspective)?
Logical Effort

<table>
<thead>
<tr>
<th>Gate Type</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>n</th>
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</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NAND</td>
<td>4/3</td>
<td>5/3</td>
<td>(n + 2)/3</td>
<td></td>
</tr>
<tr>
<td>NOR</td>
<td>5/3</td>
<td>7/3</td>
<td>(2n + 1)/3</td>
<td></td>
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<tr>
<td>Multiplexer</td>
<td>2</td>
<td>2</td>
<td></td>
<td>2</td>
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<tr>
<td>XOR</td>
<td>4</td>
<td></td>
<td>12</td>
<td></td>
</tr>
</tbody>
</table>

[From Sutherland, Sproull, Harris]
Optimizing Complex Combinational Logic
Multistage Networks

\[ \text{Delay} = \sum_{i=1}^{N} \left( p_i + \text{LE}_i f_i \right) \]

Effective fanout: \( \text{EF}_i = \text{LE}_i f_i \)

Path delay \( D = \sum d_i = \sum p_i + \sum \text{EF}_i \)

Path electrical fanout: \( F = \frac{C_L}{C_{in}} = \prod f_i \)

Path logical effort: \( \Pi \text{LE} = \text{LE}_1 \text{LE}_2 \ldots \text{LE}_N \)

Path effort: \( PE = \Pi \text{LE} F \)

Only for tree networks
Adding branching

Branching effort: \[ b = \frac{C_{L,\text{on-path}} + C_{L,\text{off-path}}}{C_{L,\text{on-path}}} \]
Multistage Networks

\[ \text{Delay} = \sum_{i=1}^{N} \left( p_i + LE_i \cdot f_i \right) \]

Effective fanout: \( EF_i = LE_i f_i \)

Path delay \( D = \Sigma d_i = \Sigma p_i + \Sigma EF_i \)

Path electrical fanout: \( F = C_L / C_{in} \)

Branching effort: \( \Pi B = b_1 b_2 \ldots b_N \)

\[ \Pi f_i = \Pi B F \quad (\text{assuming all paths in the tree are important}) \]

Path logical effort: \( \Pi LE = LE_1 LE_2 \ldots LE_N \)

Path effort: \( PE = \Pi LE \Pi B F \)
Optimum Effort per Stage

When each stage bears the same effort (effective fanout):

\[ EF^N = PE \]
\[ EF = \sqrt[1]{PE} \]

Effective fanouts: \( LE_1 f_1 = LE_2 f_2 = \ldots = LE_N f_N \)

Minimum path delay

\[ \hat{D} = \sum_{i=1}^{N} (LE_i f_i + p_i) = N \cdot PE^{\frac{1}{N}} + \sum_{i=1}^{N} p_i \]
For a given load, and given input capacitance of the first gate
Find optimal number of stages and optimal sizing

\[ D = N \cdot PE^{1/N} + \sum P_i \]

Remember: we can always add inverters to the end of the chain

The ‘best effective fanout’ \( EF = PE^{1/N} \) is still around 4
(3.6 with \( \gamma=1 \))
Method of Logical Effort: Summary

- Compute the path effort: $PE = (\Pi LE)BF$
- Find the best number of stages $N \sim \log_4 PE$
- Compute the effective fanout/stage $EF = PE^{1/N}$
- Sketch the path with this number of stages
- Work either from either end, find sizes:
  $C_{in} = C_{out} \times LE/EF$

Optimizing Complex Combinational Logic: Examples
Example 1: No branching

Electrical fanout, $F =$
$$\Pi \ LE =$$
$$PE =$$
$$EF/\text{stage} =$$
$a =$
$b =$
$c =$
Example 1: No branching

Electrical fanout, $F = 5$

$\Pi \ LE = 25/9$

$PE = 125/9$

$EF/\text{stage} = 1.93$

$a = 1.93$

$b = 2.23$

$c = 2.59$

From the back

$5/c = 1.93$

$(5/3)c/b = 1.93$

$(5/3)b/a = 1.93$

$a, b, c$ are input capacitances normalized to the unit inverter.
Our old problem: which one is better?

\[
LE = \frac{10}{3} \quad 1 \\
\Pi LE = \frac{10}{3} \\
P = 8 + 1
\]

\[
LE = 2 \quad \frac{5}{3} \\
\Pi LE = \frac{10}{3} \\
P = 4 + 2
\]

\[
LE = \frac{4}{3} \quad \frac{5}{3} \quad \frac{4}{3} \quad 1 \\
\Pi LE = \frac{80}{27} \\
P = 2 + 2 + 2 + 1
\]
Adding Branching

\[ LE = 1 \]
\[ F = \frac{90}{5} = 18 \]
\[ PE = 18 \text{ (wrong!)} \]
\[ EF_1 = \frac{(15+15)}{5} = 6 \]
\[ EF_2 = \frac{90}{15} = 6 \]
\[ PE = 36, \text{ not } 18! \]

Better: \( PE = F \cdot LE \cdot B = 18 \cdot 1 \cdot 2 = 36 \)
Select gate sizes $y$ and $z$ to minimize delay from $A$ to $B$

Logical Effort: $LE =$

Electrical Fanout: $F =$

Branching Effort: $B =$

Path Effort: $PE =$

Best Effective Fanout: $EF =$

Delay: $D =$
Select gate sizes $y$ and $z$ to minimize delay from $A$ to $B$

Logical Effort: $LE = (4/3)^3$

Electrical Fanout: $F = C_{out}/C_{in} = 9$

Branching Effort: $B = 2 \cdot 3 = 6$

Path Effort: $PE = \prod LE \cdot F \cdot B = 128$

Best Effective Fanout: $EF = PE^{1/3} \approx 5$

Delay: $D = 3 \cdot 5 + 3 \cdot 2 = 21$

Work backward for sizes:

$z = \frac{9C \cdot (4/3)}{5} = 2.4C$

$y = \frac{3z \cdot (4/3)}{5} = 1.9C$