Discussion 5

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Logical effort

- Property of the gate type (topology)
  - NAND2, NAND3, NOR2, NOR3, XOR, ...
  - The way the transistors geometrically connected decides logical effort

- Easiest way to calculate LE
  - Match the resistance of the pull-up & pull-down to unit inverter
  - Calculate $\frac{C_{in\_gate}}{C_{in\_inv}}$

- Same for intrinsic delay
Advanced example – CMOS transmission gate

• Used in tri-state buffer, multiplexers, etc.
• PMOS & NMOS are generally equally sized
• We can model the two transistors in parallel as an ideal switch with resistance equal to that of an NMOS transistor for both rising and falling transitions.
• How to calculate the logical effort of a transmission gate?
Advanced example – transmission gate

- There should always be pull-up & pull-down path from VDD/GND to define logical effort!!
- LE can be defined with a driver circuit for the transmission gate
- With an inverter,
  - LE for d: 2
  - LE for s: 4/3 (should always drive s & s’)

(a) [Diagram]

(b) [Diagram]
Advanced example – transmission gate
Applying LE for path delay calculation

• Any gate can now be treated as simple inverter, you just need to use LE as a weight factor for the fanout of that gate (F*LE=EF)

What do value a, b, c mean??
→ Absolute input capacitance, in the unit of reference inverter input capacitance

**Electrical fanout, F =**

\[
\Pi LE = PE = EF/\text{stage} = a = b = c =
\]
Applying LE for path delay calculation

Electrical fanout, $F = 5$

$\Pi \ LE = 25/9$

$PE = 125/9$

$EF/\text{stage} = 1.93$

$a = 1.93$

$b = 2.23$

$c = 2.59$

From the back

$5/c = 1.93$

$(5/3)c/b = 1.93$

$(5/3)b/a = 1.93$
Easy way to think of power dissipation

- You burn power only at pull-up transition
- Cap charge: 0 -> CVdd (C)
Easy way to think of power dissipation

- Electrical work: \( W = Q \int_a^b \mathbf{E} \cdot d\mathbf{r} \)
- From power source (Vdd) perspective: \( \int (\mathbf{E} \cdot d\mathbf{r}) = Vdd \) (constant)
- Therefore, \( W = QVdd = CVdd^2 \)
Reviewing the basics

- Resistors in parallel: \( R = \frac{R_1 \times R_2}{R_1 + R_2} \)
- Resistors in series: \( R = R_1 + R_2 \)
- Capacitors in parallel: \( C = C_1 + C_2 \)
- Capacitors in series: \( C = \frac{C_1 \times C_2}{C_1 + C_2} \)
- \( Q = CV \)
- \( i = C \frac{dv}{dt} \) (from \( i = \frac{dq}{dt} \), take \( \frac{d}{dt} \) of \( Q = CV \))
- Stored energy is work required to charge it. \( v = \frac{q}{C}, \ dw = \frac{v \ dq}{C} = \frac{dq}{C}, \) integrate to find \( E = Q^2 / (2C) \)
- Or \( E_{\text{stored}} = \frac{1}{2} C v^2 = \frac{1}{2} QV \) (from \( E = \int(P \ dt) \), plug in \( P = IV \) and \( I = C \frac{dv}{dt} \))
- Transistor \( C = C \times W, R = R / W \)...Doubling width of transistor halves the resistance and doubles the capacitance
Reviewing the basics

- $P=IV$ (power is product of voltage and current) ...Watts
- $E=PT$ (energy is power integrated over interval $T$) = $\int vi\, dt$ ...Joules = Watt*seconds.
  - 1 Watt*hour = 3600 Watt*seconds
- $V=IR$ (ohms law)
- $P=i^2R=v^2/R$
Things you need to know

• Draw a VTC for a given gate
• Describe the interesting points in a VTC. How is VIH and VIL defined? What is the noise margin and why does it matter?
• Switch model for an NMOS and PMOS. When is it on? Off?
• Implement arbitrary CMOS logic gates (PUN, PDN)
• Draw CMOS implementations of NAND/NOR/INV/
• How can transmission gates be used?
• What are tri-state buffers?
• Draw a switch model of a gate
• Size a gate to balance rise/fall times
• Draw the capacitances associated with a CMOS gate
• Translate RC network to delay
Things you need to know

• How do you optimize a variable?
• Redo the inverter chain optimal delay proof
• What is the optimal effective fanout? Why?
• Is it better for the fanout to be too high or too low?
• Trade-off between fanout and number of stages
  • Logical effort of common gates
  • Derive the logical effort for an arbitrary gate
  • Translate logical effort to delay
  • Solve for delay of network with different gates, fanout, branching. Optimize this delay
Things you need to know

• Where does the capacitance come from
• How does capacitive coupling work?
• Calculate resistance from sheet resistance
• RC models for interconnect
• Calculate Elmore delay of a network
• Derive tau for a wire
• Delay for lumped vs. distributed RC
• Derivation of delay from step on an RC circuit (where 0.69 comes from)
• How many repeaters do you need?
Things you need to know

- Instantaneous vs. peak vs. average power
- Derivation of energy drawn from the supply vs. stored on a capacitor
- Use switch model/results of derivation to calculate how much energy is drawn/stored on a capacitor
- **What is short circuit current. More common on big load or small load?**
- Find power based on capacitance, frequency and activity
- Convert between power and energy
- What is glitching?
- Describe a simple current model for a transistor (beyond the switch model)
- How does parallelism and pipe-lining help power?