MOS Switch

MOS Transistor

A Switch!

\[ V_{GS} \geq V_T \]

\[ R_{on} \]
MOS Switch

ON/OFF Model

\[ V_{GS} < V_T \]

\[ V_{GS} \geq V_T \]

“More Realistic” Model

\[ V_{GS} \geq V_T \]

\[ V_{GS} < V_T \]
MOS Switch

- Source of NMOS always at lower voltage
- Source of PMOS always at higher voltage
- The ‘effective’ source node can change depending on the voltage at the MOS’ terminals
Switch Logic

What does this circuit do?
CMOS Logic

\[ \text{OUT} = \overline{A \cdot B} \]

PUN and PDN are dual logic networks
PUN and PDN functions are complementary
CMOS Inverter

Schematic:
- $V_{DD}$
- $W_{p/L}$
- $W_{n/L}$
- $M_1$
- $M_2$
- $A$
- $G$
- $S$
- $D$
- $Out$

Truth Table:
- $V_{in} = V_{DD}$: $V_{out} = 0$
- $V_{in} = 0$: $V_{out} = V_{DD}$

Graph:
- $V_{Out}$
- $V_{DD}$
- $V_{DD}/2$
- $0$, $V_{IL}$, $V_{IH}$, $V_{DD}$
- Switching point

$V_{OL} = 0$
$V_{OH} = V_{DD}$
Inverter Sizing

- \( R_{\text{on}} \) of each FET is inversely proportional to its width
- Assume \( V_{\text{th,n}} = V_{\text{th,p}} \)
- Assume \( R_{\text{on,n}} = R_{\text{on,p}} \) for the same width unless otherwise specified
- \( W_p = W_n = \) switching threshold of \( V_{dd}/2 \)
- If \( W_p \gg W_n \), \( V_m \) approaches \( V_{DD} \)
- If \( W_n \gg W_p \), \( V_m \) approaches 0
Inverter Sizing

- Cin (gate input capacitance) and Cp (intrinsic drain capacitance) are proportional to W
  - You may see Cp referred to Cd in other sources
  - \( Cp = \gamma \) Cin
- How does the inverter delay change if either PMOS/NMOS width is doubled?
- If both widths are doubled, does the intrinsic (unloaded) delay improve?
- Inverters are usually sized to equalize high→low and low→high delays
Inverter RC Delay (High \rightarrow Low)

- High to low output transition time governed by strength of NMOS pulling low
- Can lower the time constant by increasing the NMOS width
Inverter RC Delay (Low -> High)

- Low to high output transition time governed by strength of PMOS pulling high
- Can lower the time constant by increasing the PMOS width

\[ V_{out} = V_{DD} (1 - e^{-\frac{t}{\tau}}) \]

\[ t_{p,\text{LH}} = (\ln 2) \tau = 0.7 R_{\text{eq,p}} (C_p + C_L) \]
LTSpice Simulation Examples
Questions