Problem 1: 3-bit Down Counter

Consider the design of a 3-bit binary down-counter. Of course, one way to implement this circuit would be with the use of a subtractor. However, as we showed in lecture for the binary up-counter, a dedicated down-counter circuit can be simpler than one using a subtractor.

Show your steps in designing a dedicated down-counter and the resulting circuit.

Solution:

Problem 2: 2-bit Sequence Counter

Consider the design of a 2-bit counter with the following sequence: 00, 11, 10, 01, 00, 11, ...

Design and show the circuit diagram for this counter.

Solution:
Problem 3: Shifter Circuit Timing

For the parallel to serial shifter circuit shown above, assume the following timing specifications:

- $t_{clk-q,max} = 10$ ps
- $t_{clk-q,min} = 8$ ps
- $t_{setup} = 10$ ps
- $t_{hold} = 5$ ps
- $t_{mux,max} = 5$ ps
- $t_{mux,min} = 4$ ps

(a) What is the maximum clock frequency for this circuit?
(b) Is there a potential hold time violation?

Solution:

\[
\frac{1}{f_{\text{clk, max}}} = t_{\text{clk, min}} = t_{\text{clk-q, max}} + t_{\text{mux, max}} + t_{\text{setup}} = 10 + 5 + 10 = 25 \text{ ps}
\]

\[f_{\text{clk, max}} = \frac{1}{25 \text{ ps}} = 40 \text{ GHz}\]

There is no hold time violation.

(c) Now assume there is clock skew of worst-case 8 ps. Now what is the maximum clock frequency? Is there now a potential hold time violation?

Solution:

Worst-case skew reduces the maximum clock frequency.

\[
\frac{1}{f_{\text{clk, max}}} = t_{\text{clk, min}} = t_{\text{clk-q, max}} + t_{\text{mux, max}} + t_{\text{setup}} + t_{\text{skew}} = 10 + 5 + 10 + 8 = 33 \text{ ps}
\]

\[f_{\text{clk, max}} = \frac{1}{33 \text{ ps}} = 30.3 \text{ GHz}\]

Skew also affects hold time constraints.

\[t_{\text{clk-q, min}} + t_{\text{mux, min}} > t_{\text{hold}} + t_{\text{skew}}\]

\[8 + 4 > 5 + 8\]

\[12 > 13\]

There is now a potential hold time violation.
Problem 4: Arithmetic Right-Shifter

Suppose you are given a 4-to-1 multiplexor. Use instances of it to show how you would implement a 4-bit wide arithmetic right-shifter.

Solution:

Problem 5: Bonding Wires

Suppose a chip is connected to its package using 4 mm long bonding wires with an inductance of 1 nH/mm. The chip operates at 1 GHz and draws 10 A at 1 V over a period of 100 ps.

How many bonding wires are needed to maintain a $V_{DD}$ supply noise spike of less than 10%?

Solution:

Adding more bonding wires in parallel decreases the effective wire inductance. You can also think about this as dividing down the current to reduce the voltage spikes.

$$L_{eff} = \frac{L_w}{n_w}$$

The largest voltage spike on the supply can be expressed as

$$V_{spike} = \frac{L_w}{n_w} \frac{dI}{dt} = \frac{4 \text{nH} \times 10 \text{A}}{n_w \times 100 \text{ps}} = 0.1 \text{V}$$

$$n_w = 4000$$