Problem 1: Basic IC Processing

Consider the simple planar IC process presented in lecture. Assuming that the NMOS transistors are fabricated in the bulk wafer substrate and the PMOS transistors are fabricated in an "n-well" (a deeply diffused region), list the set of masks that would be need to fabricate circuits involving both NMOS and PMOS transistors and their interconnections using one layer of metal.

Problem 2: MOS Transistor Operation

For the following parts, submit a screen shot of your circuit schematic and plots.

(a) Using LTSpice, determine $I_{off}$ and $I_{on}$ of an NMOS transistor for $L = 16$ nm and $W = 1$ µm using the provided process technology.

(b) Using LTSpice, demonstrate the dependence of transistor width on $I_{on}$ using the provided process technology. (Hint: you will want to do part (a) with a parametric sweep). What is the relationship between $W$ and $I_{on}$?

(c) 251A only — Optional Challenge Question for 151

Using LTSpice, answer and demonstrate the following:

(i) Do transistors in parallel really act as one "wide" transistor when switching a load $C$? Offer an explanation for your results.

(ii) Do transistors in series really act as one "long" transistor when switching a load $C$? Offer an explanation for your results.

Problem 3: Transistor Model

In class, we modeled a MOSFET as a switch with some resistance. Use LTSpice to find the equivalent on resistance $R_{on}$ of an NMOS transistor for $L = 16$ nm and $W = 1$ µm. Run a transient simulation with the NMOS gate initially at 0 V and the drain connected to a 1 nF capacitor to GND, with the capacitor’s voltage initially at $V_{DD}$. Step the gate voltage from 0 to $V_{DD}$ and use $\tau$ to determine $R_{on}$.
Problem 4: Cascaded "AND" Gates

Assume you ignore the rules about pmos only pullup networks and nmos only pulldown networks, and build an AND gate using 4 transistors, shown below.

Note that there is only one input and the unused inputs are 1's.

Next you cascade 3 of these gates and label each gate output node as $a$, $b$, and $c$ respectively. Initially $a$, $b$, and $c$ are all 0 volts. Transition the input from 0 to 1. Draw the waveforms at $a$, $b$, and $c$. Assume that $V_{th} = \frac{1}{2}V_{DD}$.

Problem 5: Transistor Level Implementation of Logic Function without Complements

Assuming that only uncomplemented inputs are available, draw a complementary static CMOS gate that implements $F = (a + b + c)' + (d + e + f)' + g'$, using the minimum number of transistors.

Problem 6: Transistor Level Implementation of Logic Function

Assuming that both complemented and uncomplemented inputs are available, draw a complementary static CMOS gate that implements $F = abd + a\overline{b}e + acf + ac\overline{g}$, using the minimum number of transistors.
Problem 7: Transmission Gate Circuits

What is the function of the circuit below? Write out the logic equations of $\text{OUT1}$ and $\text{OUT2}$.