# **Discussion Section 11**

Sean Huang April 16, 2021



#### **Counter Blocks**

- Simple to implement
  - Just an add 1 every clock cycle!
- Register to remember the count





#### **Counter Blocks**

- Simple to implement
  - Just an add 1 every clock cycle!
- Register to remember the count
- Adders are expensive
  - Too general
  - Do we really need an entire adder to just count by 1 each time?





#### **Counter Blocks**

- Determine next value combinationally
- Use the same tools as encoding state machines to design next count logic
  - K-maps, Boolean algebra, Truth tables

а	b	С	d	a'	b'	с'	d'
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	1	1	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	1	0
1	1	1	0	1	1	1	1
1	1	1	1	0	0	0	0



#### Terminal Count (tc)

- Common output of counters
- Flag set when either the counter reaches its maximum/minimum value or a set threshold value
- Useful for using counters in state machines



## **Booth Recoding**

- Do partial products every 2 bits instead of 1 for fewer operations
- Traditional partial products
  - 0
  - A
- Higher-radix has more partial products
  - 0
  - A
  - 2A
  - 3A

B <sub>k+1</sub>	<b>B</b> <sub>k</sub>	B <sub>k-1</sub>	Action
0	0	0	Add 0
0	0	1	Add A
0	1	0	Add A
0	1	1	Add 2A
1	0	0	Sub 2A
1	0	1	Sub A
1	1	0	Sub A
1	1	1	Add 0



## **Booth Recoding**

- Higher-radix has more partial products, which we can decompose as such
  - 0 = 0
  - -A = A
  - -2A = 4A 2A
  - 3A = 4A A
- 4A is simply A shifted 2 to the left, so this is the same as adding A to the next partial sum

B <sub>k+1</sub>	B <sub>k</sub>	B <sub>k-1</sub>	Action
0	0	0	Add 0
0	0	1	Add A
0	1	0	Add A
0	1	1	Add 2A
1	0	0	Sub 2A
1	0	1	Sub A
1	1	0	Sub A
1	1	1	Add 0



#### **Booth Recoding Example**

- For first bit pair, implied  $B_{k-1}=0$
- First pair is 11,  $B_{k-1}=0$ 
  - Perform 4A A
  - Put down -A for this partial product

11[0]

Sub A

For first bit pair assume previous pair is 00





#### **Booth Recoding Example**

- For first bit pair, implied  $B_{k-1}=0$
- First pair is 11,  $B_{k-1}=0$ 
  - Perform 4A A
  - Put down -A for this partial product
- Next pair is 10,  $B_{k-1}=1$ 
  - Perform 4A 2A
  - Put down -A (-2A + A from last partial)

11[0] Sub A 10[1] Sub A







#### **Booth Recoding Example**

- For first bit pair, implied  $B_{k-1}=0$
- First pair is 11,  $B_{k-1}=0$ 
  - Perform 4A A
  - Put down -A for this partial product
- Next pair is 10,  $B_{k-1}=1$ 
  - Perform 4A 2A
  - Put down -A (-2A + A from last partial)
- Last pair 01,  $B_{k-1}=1$ 
  - Perform +2A

× 01101100 11[0] Sub A -010101 10[1] Sub A -010101 01[1] Add 2A +010101

01000110111

For first bit pair assume

previous pair is 00

010101



• Booth recoding does not really work well for signed multiplication



 Must sign extend and subtract last partial for signed multiplication  $\begin{array}{r} a_{3}a_{2}a_{1}a_{0} \\ \times b_{3}b_{2}b_{1}b_{0} \\ a_{3}b_{0} \ a_{3}b_{0} \ a_{3}b_{0} \ a_{3}b_{0} \ a_{3}b_{0} \ a_{2}b_{0} \ a_{1}b_{0} \ a_{0}b_{0} \\ + a_{3}b_{1} \ a_{3}b_{1} \ a_{3}b_{1} \ a_{3}b_{1} \ a_{2}b_{1} \ a_{1}b_{1} \ a_{0}b_{1} \\ + a_{3}b_{2} \ a_{3}b_{2} \ a_{3}b_{2} \ a_{2}b_{2} \ a_{1}b_{2} \ a_{0}b_{2} \\ - a_{3}b_{3} \ a_{3}b_{3} \ a_{2}b_{3} \ a_{1}b_{3} \ a_{0}b_{3} \end{array}$ 



- Must sign extend and subtract last partial for signed multiplication
- Can remove sign extension by adding a 1 at the MSB of each partial product
- $a_3 a_2 a_1 a_0$  $\times b_3 b_2 b_1 b_0$  $a_3b_0 a_3b_0 a_3b_0 a_3b_0 a_3b_0 a_2b_0 a_1b_0 a_0b_0$  $+ a_3b_1 a_3b_1 a_3b_1 a_3b_1 a_2b_1 a_1b_1 a_0b_1$ +1 $+ a_{3}b_{2} a_{3}b_{2} a_{3}b_{2} a_{2}b_{2} a_{1}b_{2} a_{0}b_{2}$  $-a_3b_3a_3b_3a_2b_3a_1b_3a_0b_3$ +1  $C_{2}$ C₄ C<sub>0</sub>



╋

+

- Must sign extend and subtract last partial for signed multiplication
- Can remove sign extension by adding a 1 at the MSB of each partial product
- Remember to subtract this constant at the end!



╋

+

+

- Must sign extend and subtract last partial for signed multiplication
- Can remove sign extension by adding a 1 at the MSB of +each partial product
- Remember to subtract this constant at the end!
- Subtraction at the end can be re-represented

 $a_3 a_2 a_1 a_0$  $\times b_3 b_2 b_1 b_0$  $\begin{array}{c} \overline{a_3b_0} & a_2b_0 & a_1b_0 & a_0b_0 \\ \hline a_3b_1 & a_2b_1 & a_1b_1 & a_0b_1 \end{array}$  $a_3b_2 a_2b_2 a_1b_2 a_0b_2$  $\overline{a_3b_3} \overline{a_2b_3} \overline{a_1b_3} \overline{a_0b_3} \setminus 2'_{s \text{ complement}}$ -A = ~A + 1 1 1 1  $C_7$  $C_4$ C<sub>3</sub>  $C_0$ 



╋

+

+

+

- Must sign extend and subtract last partial for signed multiplication
- Can remove sign extension by adding a 1 at the MSB of each partial product
- Remember to subtract this constant at the end!
- Subtraction at the end can be re-represented

 $a_3 a_2 a_1 a_0$  $\times b_{3}b_{2}b_{1}b_{0}$  $\begin{array}{c} \overline{a_3 b_0} & a_2 b_0 & a_1 b_0 & a_0 b_0 \\ \hline a_3 b_1 & a_2 b_1 & a_1 b_1 & a_0 b_1 \end{array} \end{array}$  $a_3b_2 a_2b_2 a_1b_2 a_0b_2$  $\overline{a_3b_3} \overline{a_2b_3} \overline{a_1b_3} \overline{a_0b_3}$ 2's complement -A = ~A + 1  $C_7$ C<sub>⊿</sub> C<sub>2</sub>





Why the sign extension can be ignored in Baugh–Wooley



• Consider both the case of a negative (2's complement) and positive number

#### **1**01001

001001



- Consider both the case of a negative (2's complement) and positive number
- Sign extend by a few bits

#### 1111111111111101001

#### 



- Consider both the case of a negative (2's complement) and positive number
- Sign extend by a few bits
- Add 1 at the original sign bit





- In the positive case
  - Extension all 0, can ignore all except inverted sign bit
- In the negative case
  - 1 carries to next sign extension bit
  - Carry chains all the way until all sign extension bits are 0
  - Drop carry out (won't affect final sum)



101001 +1



- In the positive case
  - Extension all 0, can ignore all except inverted sign bit
- In the negative case
  - 1 carries to next sign extension bit
  - Carry chains all the way until all sign extension bits are 0
  - Drop carry out (won't affect final sum)



101001 +1

