Discussion Section 5

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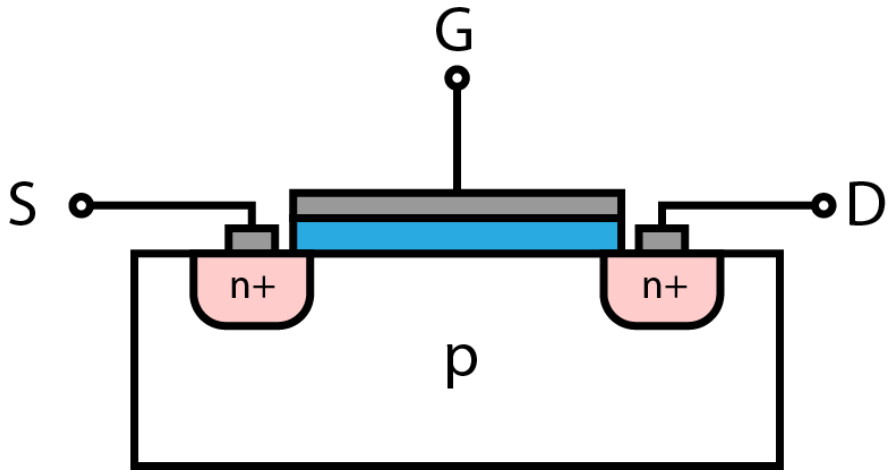
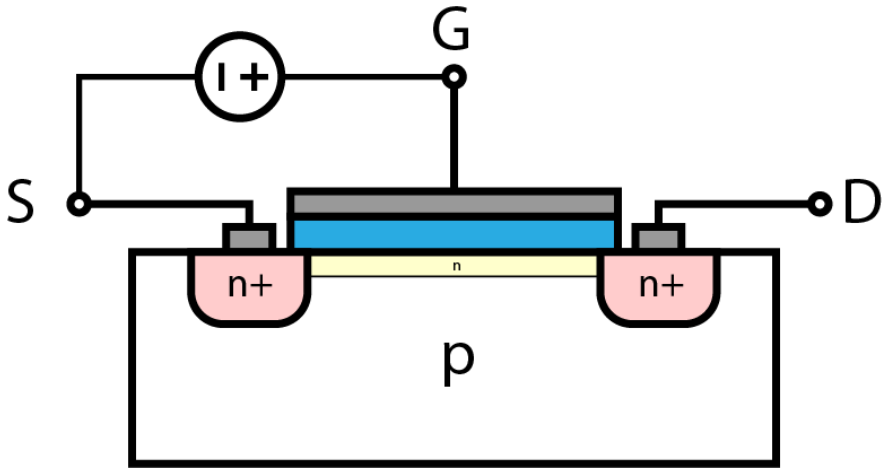
MOS Basics

- Used to be made in a planar process
- Wafer is usually p-doped
- 3 main contacts
  - Gate
  - Source
  - Drain
- Gate controls current flow from Source to Drain

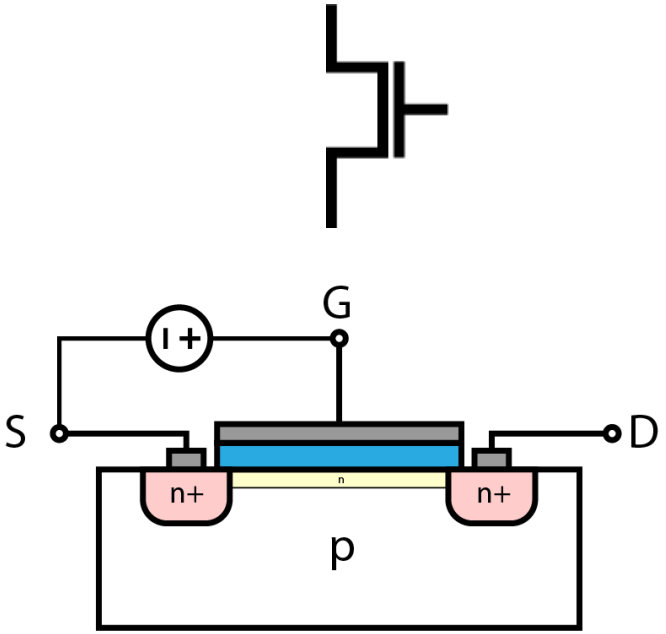


MOS Basics

- MOS turns “on” when voltage applied across gate-source
- Voltage causes top layer of silicon to invert types, connecting S to D

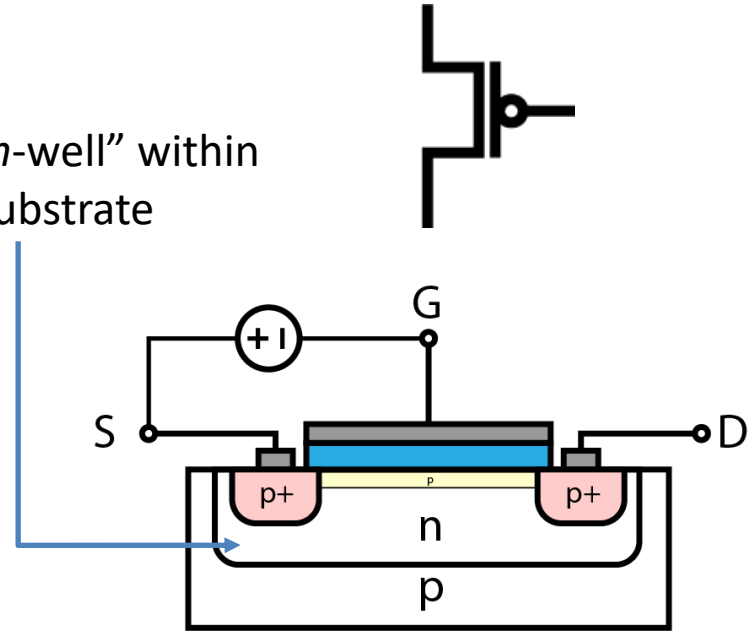


MOS Basics



NMOS (n-type FET, nFET)
Turns on when gate input = 1
Source at lowest voltage

Notice the "*n*-well" within the *p*-substrate



PMOS (p-type FET, pFET)
Turns on when gate input = 0
Source at highest voltage

MOS Basics

Can approximate these as a switch with some series resistance

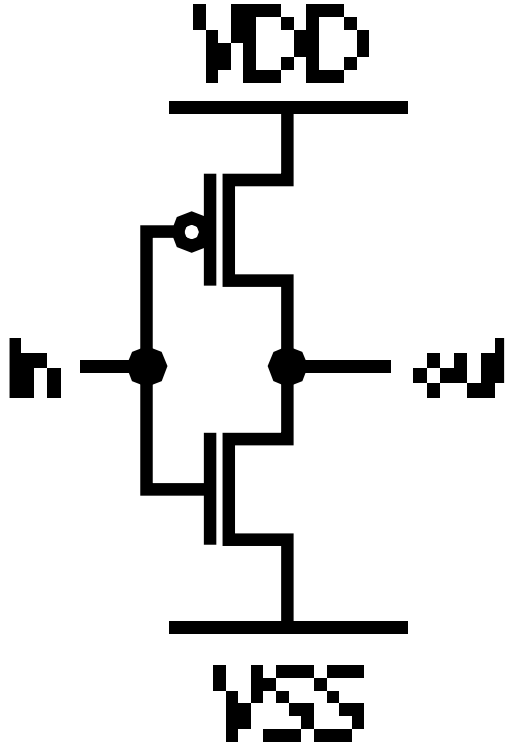
MOS Basics

Can approximate these as a switch with some series resistance

Terminals have capacitance

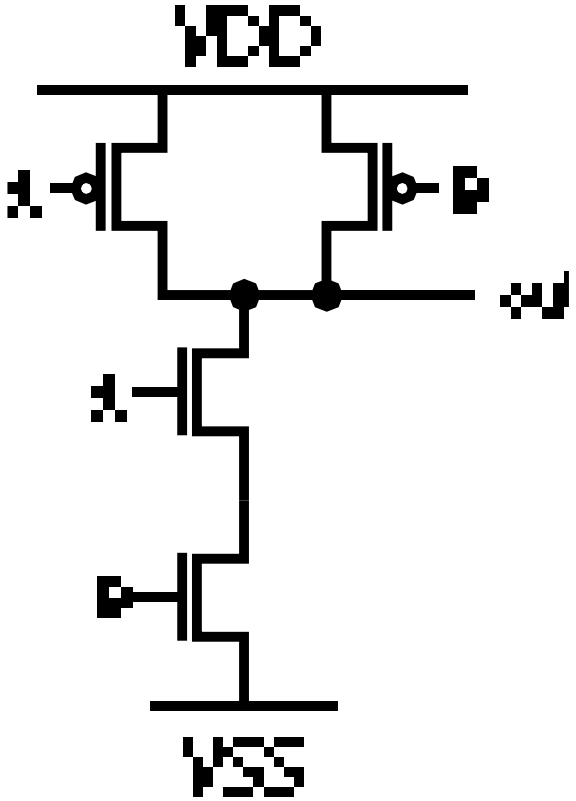
Complementary MOS (CMOS)

- PMOS and NMOS have *complementary* functions
  - Have one pull up and other pull down
- Together this makes an inverter
  - When input is 0, NMOS off, PMOS on
    - PMOS pulls output to 1
  - When input is 1, NMOS on, PMOS off
    - NMOS pulls output to 0



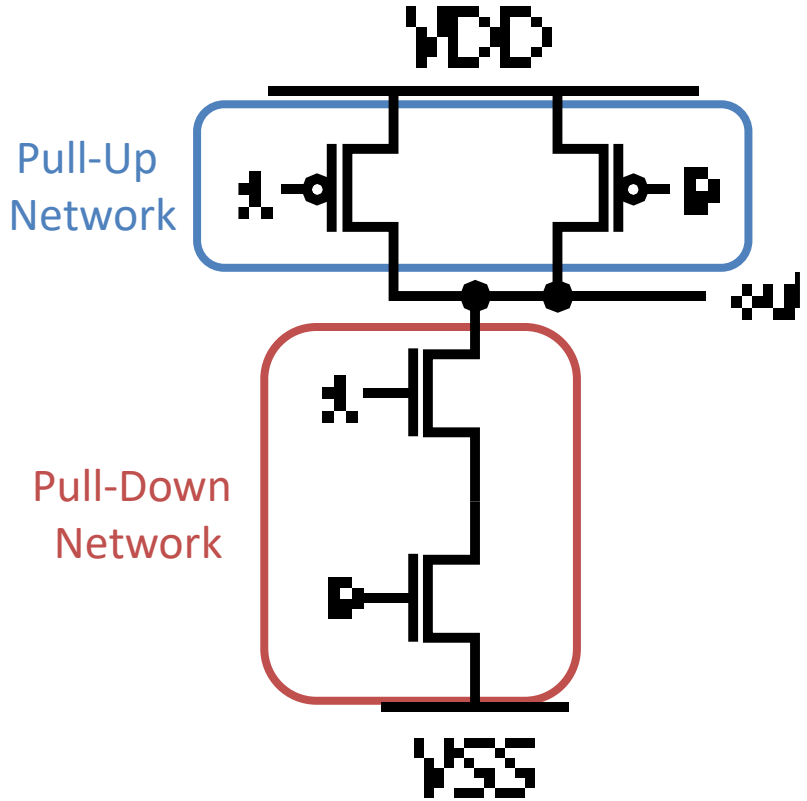
Complementary MOS (CMOS)

- Multiple inputs by adding devices
  - 2-NAND example
- Note NMOS and PMOS networks look different
  - Out = 1 unless both inputs are 1
  - Either PMOS can pull output to 1
  - Both NMOS must be on to pull down to 0



Complementary MOS (CMOS)

- PMOS network called *Pull–Up Network (PUN)*
- NMOS network called *Pull–Down Network (PDN)*
- Networks are duals are *always* complementary
  - Parallel PUN
  - Series PDN

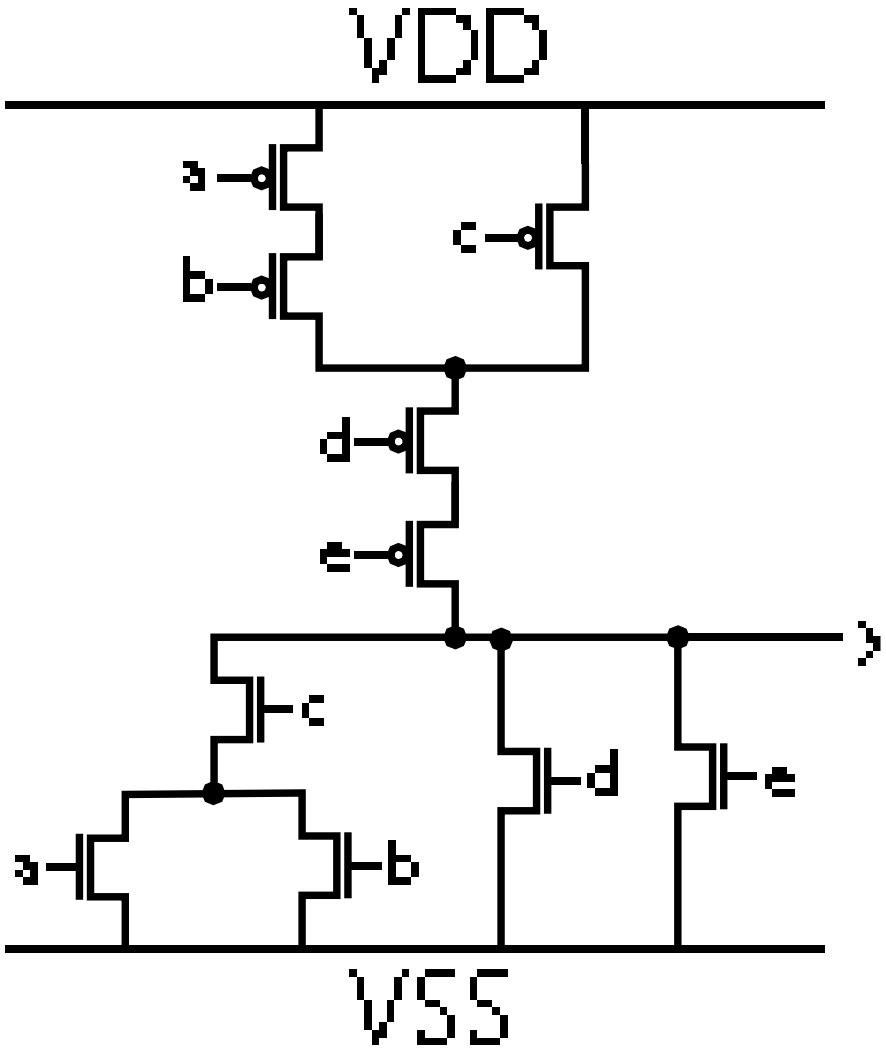


Complex CMOS

- CMOS circuits not limited to simple logic functions
  - Can implement any logic function using complementary networks
- What function is implemented here?

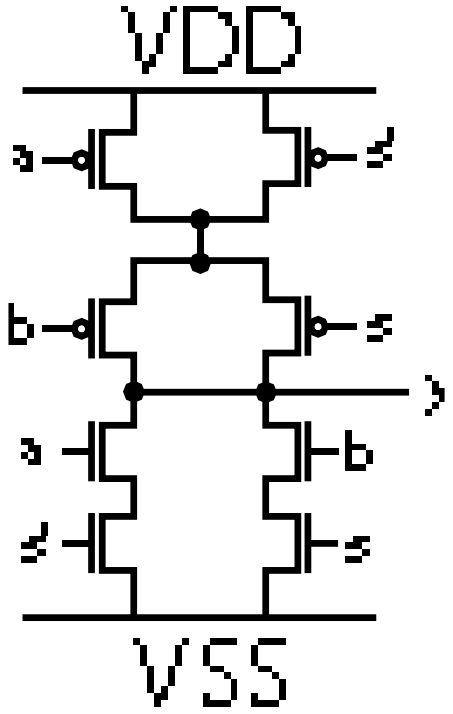
$$y = ((a + b)c) + d + e$$

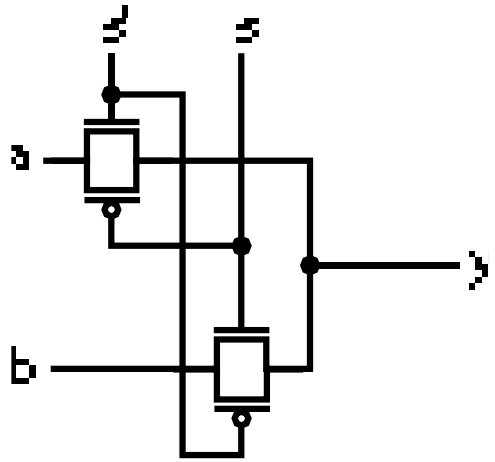
$$y = (a'b' + c')d'e'$$



Static vs. xGate Logic

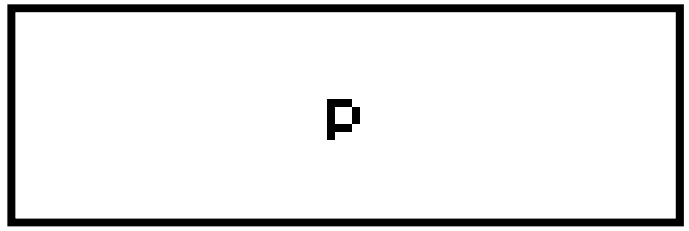
- Two main flavors of CMOS logic
- Static Logic
  - Output always connected to either VDD or VSS within gate
  - Output always 1 or 0
- Transmission-gate (xGate) Logic
  - Output connected to inputs, but not to supplies within gate
  - Cannot drive output without an input





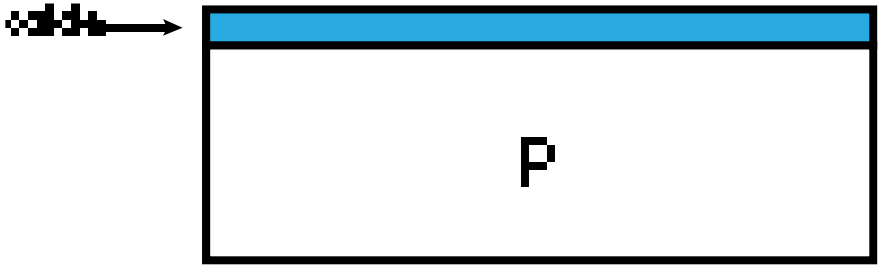
Photolitography

- Wafers generally start p-doped



Photolitography

- Wafers generally start p-doped
- Oxide grown by baking in oven with O_2



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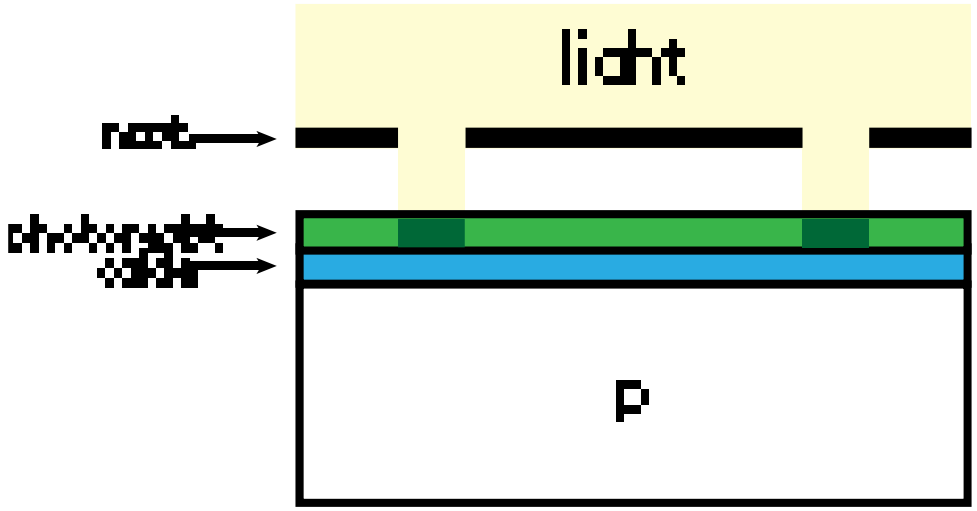

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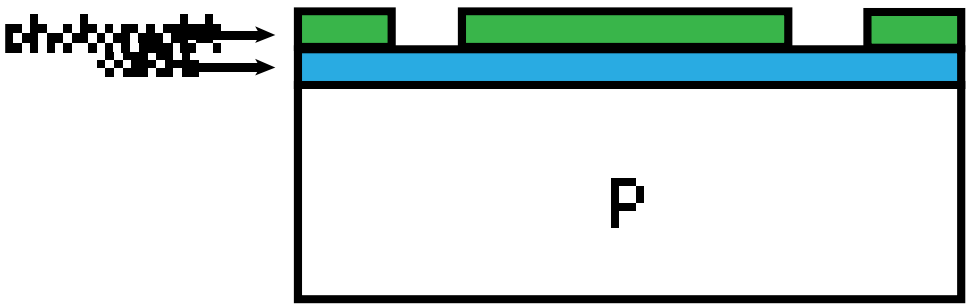
- Develop photoresist



Photolitography

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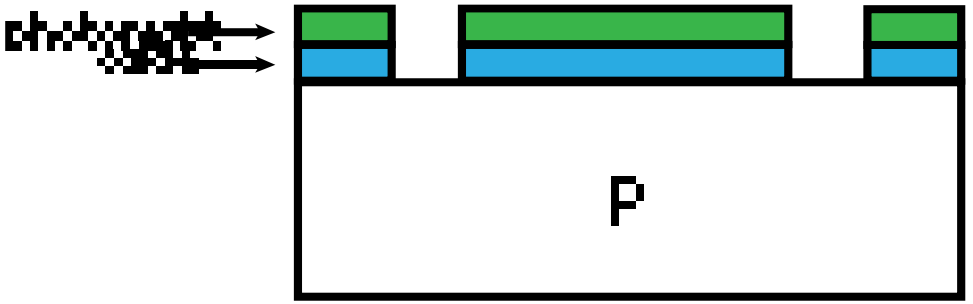
- Oxide grown by baking in oven with O_2
- Apply photoresist at beginning of lithography process
- Expose photoresist to light with pattern mask
- Develop photoresist
- Etch oxide



Photolitography

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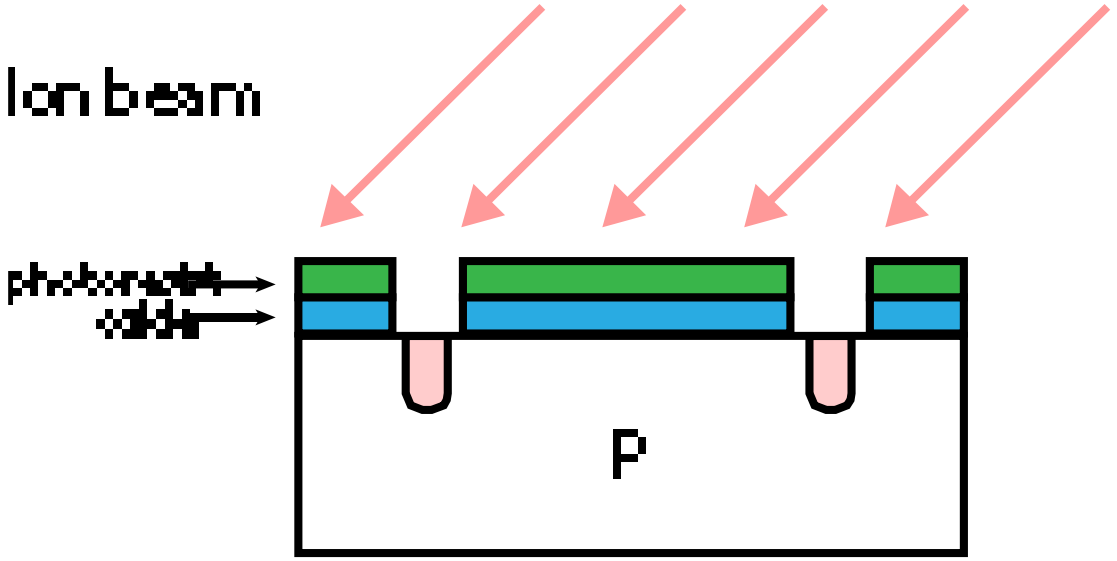
- Apply photoresist at beginning of lithography process
- Expose photoresist to light with pattern mask
- Develop photoresist
- Etch oxide
- Implant ions



Photolitography

- Wafers generally start p-doped
- Oxide grown by baking in oven with O_2
- Apply photoresist at beginning of lithography process
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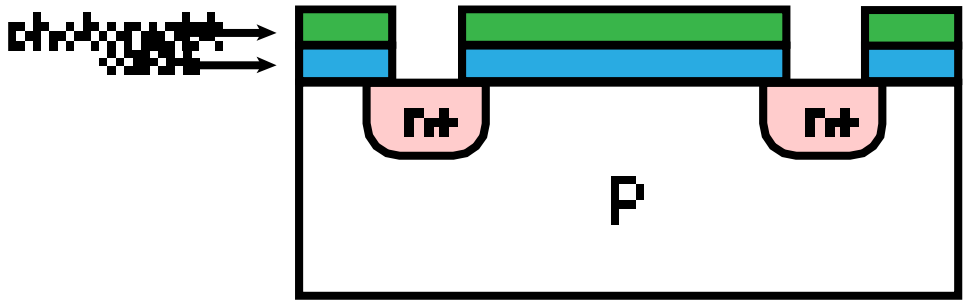
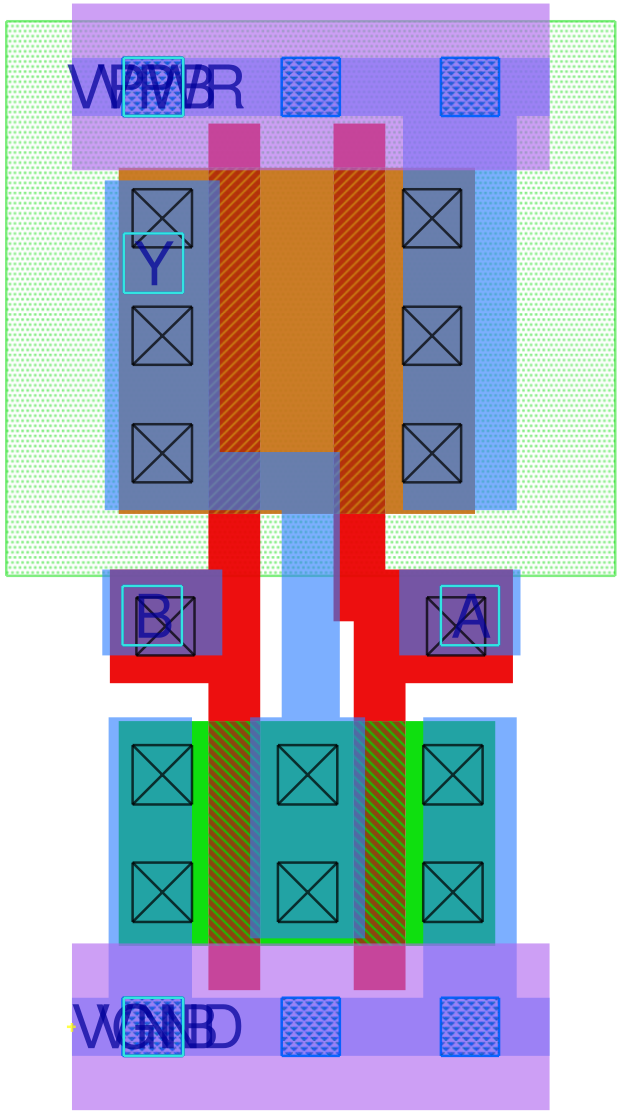
- Develop photoresist
- Etch oxide
- Implant ions
- Anneal

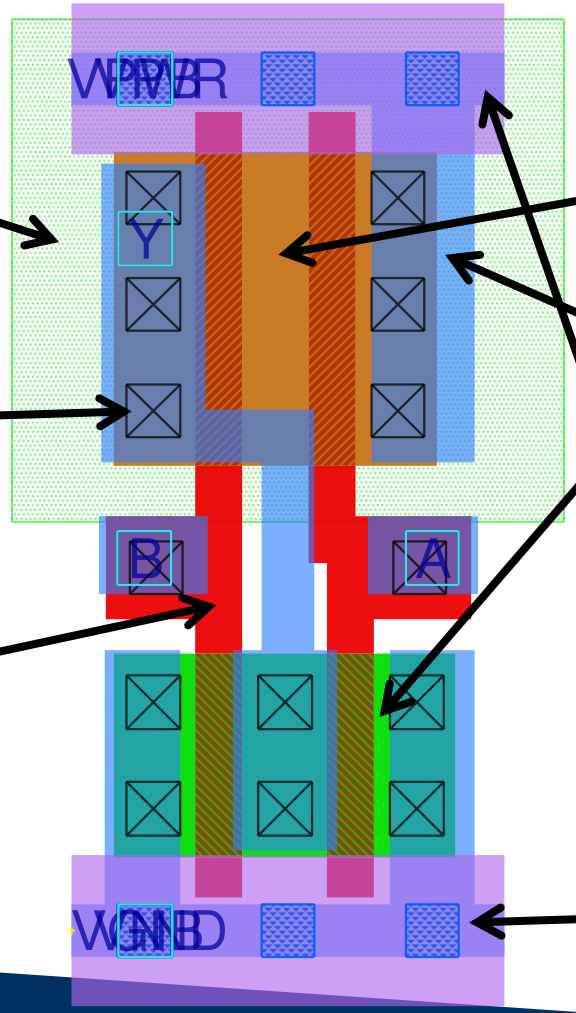


Standard Cell Layout

- Provided by foundry in a Development Kit
- Usually a library of common logic gates
- Designed to be easy to tile and put together with place and route tools
  - Standard height within the same process
  - Taller cells made in multiples of minimum row height
  - Power rails easy to connect together
  - Many design rules already followed and abstracted away by the cell



Important Features



n-well: required for making PMOS devices

Vias: vertical connection between layers

Polysilicon: gate connection. Pins connected to the gate will connect to this layer

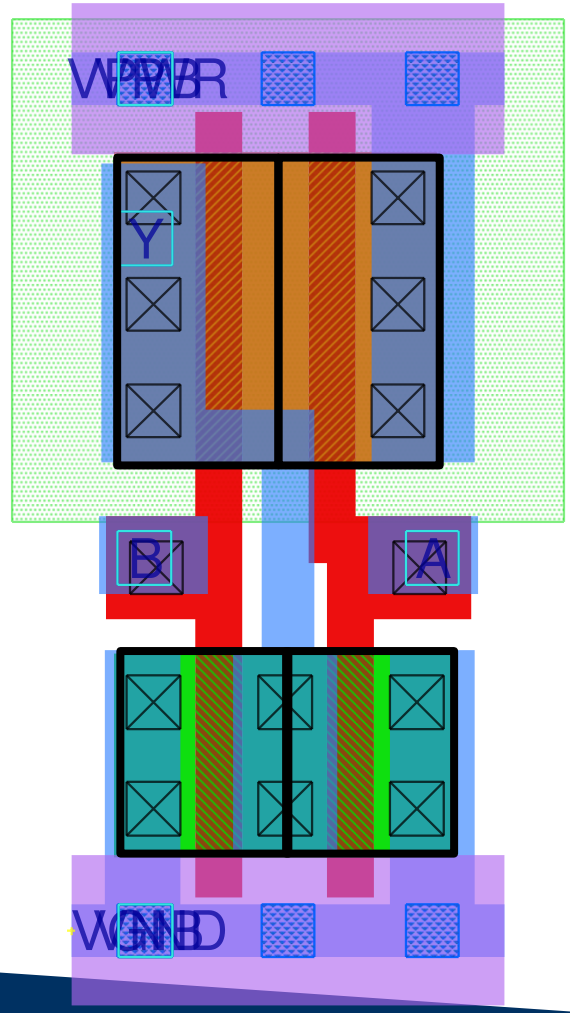
Diffusion region: represents the source/drain contact areas of the transistor

Metal Routing: metal wires in layout

Power Rails: VDD and VSS supply rails for the cell

Transistors

Each diffusion-poly-diffusion group is a transistor

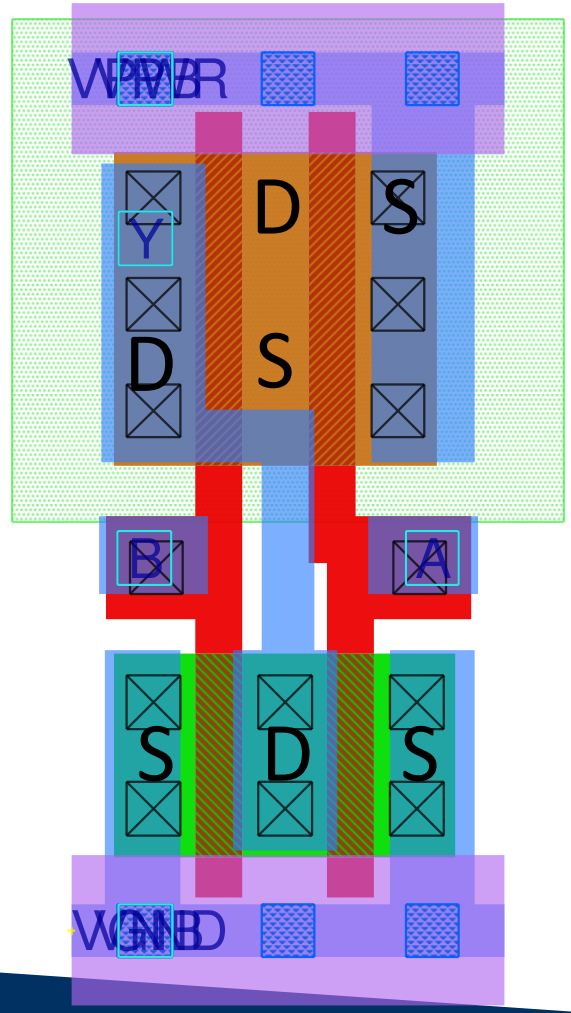


These devices must be PMOS because they are within the n-well

Each diffusion-poly-diffusion group is a transistor

These devices are not in the n-well, and therefore are NMOS

Transistors



One transistor's drain could be another transistor's source

Either side of poly (Gate) is the Source or Drain

Transistors can "overlap" and share sources/drains

Standard Cell Layout Analysis

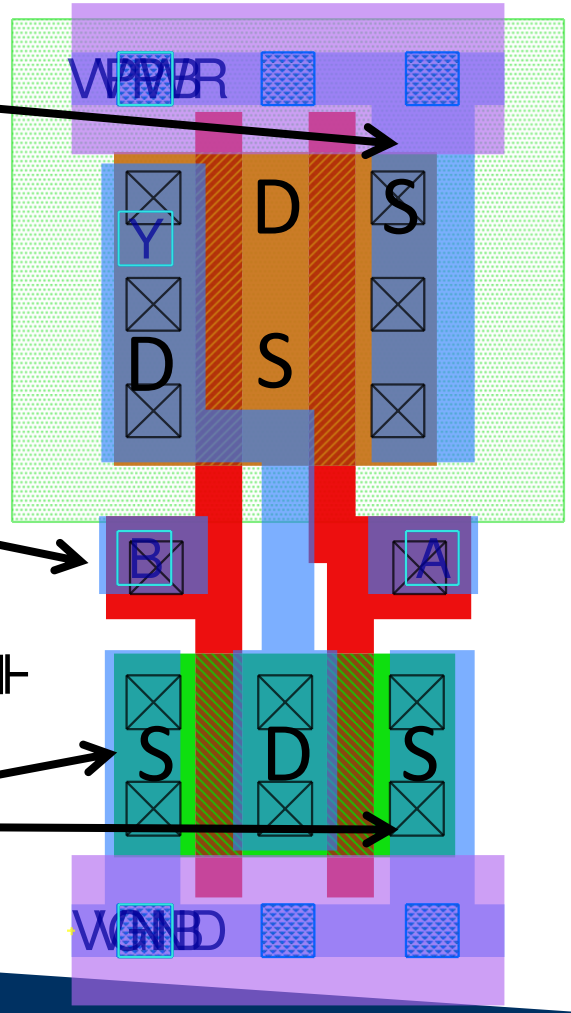
The source of this device is connected to VDD

The drain of one device here becomes the source of the next device, so these are in series.

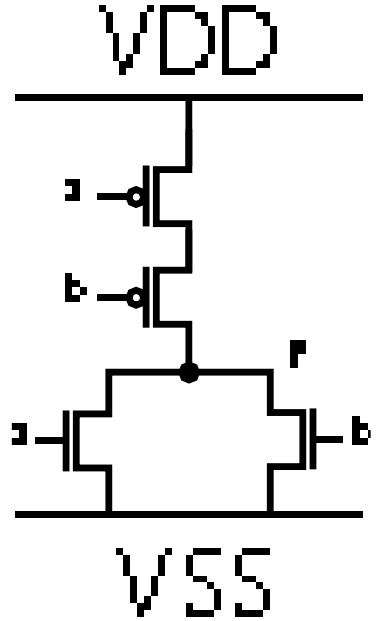
The poly (gate) connections for both transistors are shared

These two transistors share a drain and a metal wire taps out from it, so these devices are in parallel

The sources of these devices are connected to VSS



Put all this together and we can work out the CMOS circuit in this cell



This is a 2-input NOR gate!